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# PIXEL DETECTOR DESIGNED IN SOI CMOS TECHNOLOGY

Disertation thesis

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# Declaration

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In Prague, February 2022

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# Abstract

This work presents development of special class of the Monolithic Active Pixel Sensors (MAPS) sensor which is fabricated in Silicon On Insulator (SOI) CMOS technology. Target application of the sensor is radiation imaging. The deep submicron SOI CMOS technology has long been used in many special applications, such as radiation-hardened or high-voltage integrated circuits.

This disertation thesis deals with the development of a pixel detector with front-end electronics in the deep submicron SOI CMOS technology. The proposed pixel detector is designed and in the 180 nm SOI CMOS commercial technology with the specific process. This study brings the solution to create the prototype of a pixel detector with two different pixel sizes. The first pixel size is 50 $\mu$m and the second is 100 $\mu$m. Both pixel types have identical front-end. In the ongoing prototypes, pixel detectors designed in 180 nm SOI CMOS technology have one type of sensor size integrated. The test structures are designed in various sub-microns CMOS technologies as the 180 nm SOI, 180 nm, 150 nm and 65 nm. The prototypes of the integrated circuits design includes test structures for measurement of radiation hardness which is an important criterium of the pixel detectors.

**Keywords:** Pixelated detectors and associated VLSI electronics; X-ray detectors; Front-end electronics for detector readout; Radiation damage to electronic components.

# Abstrakt

Tato práce představuje vývoj speciální třídy MAPS senzoru, který je vyroben v SOI CMOS technologii. Cílovou aplikací senzoru je radiační zobrazování. Hluboká submikronová technologie submicron SOI CMOS se již dlouho používá v mnoha speciálních aplikacích, jako jsou radiačně odolné nebo vysokonapěťové integrované obvody.

Tato disertační práce se zabývá vývojem pixelového detektoru s front-end elektronikou v hluboké submikronové technologii SOI CMOS. Vyvinutý pixelový detektor je navržen v komerční technologii 180 nm SOI CMOS se specifickým procesem. Tato studie přináší řešení pro vytvoření prototypu pixelového detektoru se dvěma různými velikostmi pixelů. Velikost prvního pixelu je 50 $\mu$m a druhého je 100 $\mu$m. Oba typy pixelů mají identický front-end. V probíhajících prototypech mají pixelové detektory navržené v technologii 180 nm SOI CMOS integrován jeden typ velikosti pixelu. Testovací struktury jsou navrženy v různých submikrometrových technologiích CMOS jako 180 nm SOI, 180 nm, 150 nm a 65 nm. Prototypy návrhu integrovaných obvodů zahrnují testovací struktury pro měření radiační odolnosti, která je důležitým kritériem pixelových detektorů.

**Keywords:** pixelový detektor, VLSI elektronika; X-ray detektory; Front-end eletronika pro pixelové detektory; radiační poškozemí elektronických komponentů.

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# List of Acronyms

**AA** Antiproton Accumulator. 15

**AC** Antiproton Collector. 15

**AD** Antiproton Decelerator. 15

**ADC** Analog to Dicital Converter. 5, 69

**BI** Beam Intensity. 49, 50

**BOX** Burried-Oxide. 2, 18, 19

**CCD** Charge-Coupled Device. 2, 52

**CMOS** Complementary Metal–Oxide–Semiconductor. iv, v, vii, viii, xii–xiv, 1–5, 16–57, 63, 64, 68–71, 82–88

**CSA** Charge Sensitive Amplifier. xi, xii, xiv, 22–28, 66, 67, 76, 77

**DAC** Digital to Analog Converter. vii, viii, xiv, 27–29, 53, 67, 70, 71, 76, 79, 82, 85

**DNL** Differential NonLinearities. xiv, 5, 71–74, 78, 79, 81, 82, 85

**DTI** Deep Trench Insulation. xi, xii, 19, 21, 41, 42

**FPGA** Field Programmable Gate Array. xiii, 55, 56, 61, 62

**HEP** High Energy Physics. 1

**HV** High Voltage. xii, 19, 24, 25, 39, 41–43, 45, 83, 84

**HVP** High-Voltage P-well. xii, 31–38, 44

**INL** Integral NonLinearities. xiv, 5, 71–75, 78, 79, 81, 82, 85

**ISR** Intersecting Storage Rings. 9

**LEIR** Low Energy Ion Ring. 14

**LEO** Low Earth Orbit. 5, 64, 87

**LEP** Large Electron-Positron Collider. 9

**LHC** Large Hadron Collider. xi, 1, 4, 7–10, 13, 14

**LORDS** Lightweight Orbital Radiation Detection System. viii, xiii, xiv, 5, 53, 61, 63–69, 84, 87, 88

**LSI** Large Scale Integration. 17

**LVDS** Low-Voltage Differential Signaling. viii, xiii, xiv, 4, 5, 53–64, 68, 69, 84, 86–88

**LVT** Low Voltage Threshold. 71, 75, 76

**MAPS** Monolithic Active Pixel Sensors. iv, v, 1, 2, 19, 64, 83

**NBUR** N-Buried Handle Wafer Diode Module. 22, 24

**NDA** Non-Disclosure Agreement. 3

**OA** Operational Amplifier. 25

**PDH** Peak Detector Hold. xiv, 64, 66, 67

**PS** Proton Synchrotron. xi, 14, 15

**PSB** Booster rings. 14

**RHIC** Relativistic Heavy Ion Collider. 10

**SEE** Single Event Effects. 3, 17, 18

**SEU** Single Event Upset. 64

**SOI** Silicon On Insulator. iv, v, vii, viii, xiii, xiv, 1–5, 16–52, 57–59, 63, 64, 68, 83–88

**SppS** Proton-Antiproton Collider. 9, 14

**SPS** Super Proton Synchrotron. xi, 9, 14, 15

**STI** Shallow Trench Isolation. 19

**SURE** Simple USB Read-out Equipment. xi, 25, 26, 84

**TDAC** Digital to Analog Converter for Threshlod adjustment. xi, 23–25, 27, 45

**TEM** Transmission Electron Microscopy. xii, 4, 43, 46, 47, 52, 84, 87

**TID** Total Ionization Dose. 17–19, 31

**VDAC** Voltage Digital to Analog Converter. xiv, 5, 70–80, 82, 85

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# Chapter 1

# Introduction

Currently, it is difficult to find a pixel detector of ionizing radiation with the corresponding parameters at an affordable price. The selection of suitable technology is governed mainly by price per $mm^2$ of the proposed chip and technology difficulty. One of the most widespread detectors is hybrid pixel detector technology, as is described in [1], which has sufficient parameters, but it is constructed in a very complex technology – higher price. Hybrid pixel detectors are popular in High Energy Physics (HEP) experiments for tracking and vertexing. Vertex detectors using this technology have been successfully implemented in experiments at the Large Hadron Collider (LHC): ATLAS [2], CMS [3] and ALICE [4]. Hybrid pixel detectors are distinguished by their excellent spatial resolution, low noise, radiation hardness, fast read-out and small inserted mass in the detector. A hybrid pixel detector is a composition of sensor and read-out chip interconnected by a suitable technology [5]–[7]. Lower limit of the pixel size restricts the technology to bump-bonding. This approach allows an independent development of these components and more freedom in design and fabrication. On the other hand, the interconnection process represents a significant portion of a financial budged for the detector production. The main leader in applications of the hybrid pixel detectors is the Medipix collaboration at CERN. The Medipix hybrid pixel detector can be combined with different semiconductor sensors which convert the ionizing radiation directly into detectable electric signal [8], [9]. Recently, more advanced technologies became available. The integration of a sensor and the complex Complementary Metal–Oxide–Semiconductor (CMOS) front-end electronics on the same chip becomes possible. The sensor and the front-end electronics are integrated on one piece of silicon. In this detector group are included the MAPS and detectors fabricated in SOI CMOS technology.

The MAPS is an integration of a sensor and front-end electronics on the same silicon wafer, thus overcoming the interconnection issues. An additional advantage of this solution is the possibility to design small pixels with small capacitance and potentially

low noise. The MAPS can be thinned down to a thickness of several tens of $\mu$m. A thin sensor with fine pixel granularity is demanded in the future HEP experiments, for example at the future linear collider CLIC [10] or ILC [11]. The sensor requires pure, high resistivity silicon (several k$\Omega$) and high depletion voltage, while CMOS electronics is usually processed on low resistivity ($< 10\ \Omega$.cm) silicon and biased with low voltage ($<$ 2 V). The technologies adopting the desired features have not been widely available until the last decade. Nowadays, many commercial applications require technologies meeting the requirements for fabrication of the MAPS sensors. The CMOS image sensors are a typical example. In recent years, the market of the CMOS image sensors started to grow largely due to their massive integration in mobile devices. The sales of the CMOS image sensors are currently higher than the Charge-Coupled Device (CCD) [12]–[14].

This work presents development of special class of the MAPS sensor which is fabricated in SOI CMOS technology. Target application of the sensor is radiation imaging. The deep submicron SOI CMOS technology has long been used in many special applications, such as radiation-hardened or high-voltage integrated circuits. It is only in recent years that SOI has emerged as a serious contender for low-power high-performance applications [15]–[18]. The main feature of the SOI pixel detectors is the sensor location. A sensor element is implemented on handling wafer. The epitaxial layer which contains the front-end electronics is separated from the sensitive part of Burried-Oxide (BOX), a detailed description is in [19] by T. Benka and in [20]–[22]. This technology has a huge advantage in separating the front-end electronics from the sensor part while maintaining both at the same chip. The SOI CMOS technology has favorable price per mm$^2$, availability of technology in factories, competitiveness for other technologies – chiefly for pixel hybrid detectors.

# Chapter 2

# Dissertation thesis targets

For a long time, the performance of the MAPS sensors has been limited due to the absence of suitable technologies allowing the integration of a sensor and the complex deep submicron CMOS electronics on the same chip is a technological challenge. Microelectronic circuits manufactured using silicon transistors fabricated on an insulating substrate (SOI) are often used in high reliability system designs. The SOI technologies continue to be developed and applied to address radiation requirements of future generation pixel detectors in various industries. The intrinsically limited collection volume of an SOI device can reduce the impact of Single Event Effects (SEE) and transient dose radiation. The case has been made that soft error mitigation may be a motivating factor for more widespread commercial adoption of the SOI, and the commercial SOI devices to below 180 nm. Lower voltages, thinner silicon and the BOX layers, new materials in devices and over layers, and non-planar multiple gate device structures have implications for radiation effect in the SOI devices. Shorter channel lengths increase the parasitic bipolar gain, know to enhance the SEE and transient dose vulnerability in advanced SOI. Thinner BOX layers can exacerbate capacitive coupling from charge deposited in the substrate. The Modern digital SOI circuits may even be sensitive to energetic protons or electrons. With thinning of the silicon layer, the total-ionizing-dose radiation response of the BOX layer and associated interfaces, in closer proximity to the devices channel(s) becomes of increased relevance. The number of the international experimets uncontrollably rises which require the solutions in the SOI CMOS technologies. The major experiments at the international organizations CERN are: ATLAS [2], CMS [3], CLIC [10] and many others. The completed functional solutions are designed in smaller collaborations, such as the Departments of the Universities. Research result obtained with the novel MAPS detectors are often published and they are avalaible to academic community. Design details (schematics with transistor dimensions) are often kept secret within the research group. Technology details are Non-Disclosure Agreement (NDA) protected or not avalaible to

academic community at all. It is therefore understanbadle, that certain sensitive information can not be presented in this document. For the development of the pixel detector, the submicron 180 nm SOI CMOS technology has been chosen. The SOI CMOS technology allows the production with the specific process the sensor part which is located under the front-end electronics, T. Benka [19], [23]–[25]. Target application of the presented detector is X-ray imaging. Other applications of the detector are particle identification and measure the spectrum of different particles (ions, electrons and soft photons [26]). Some of these applications have been described by Z. Janoska, T. Benka et al in [27]. Nowadays, many commercial applications require technologies, which correspond the requirements for fabrication of the MAPS sensors. It may lead to new types of particle imaging detectors, for example, the upgrade of the LHC experiment, imaging detectors in medicine described by G. Neue, T. Benka et al in [28], detectors for dosimetry, G. Neue, T. Benka et al., etc. in [29]–[32]. The main advantage compared to hybrid pixel detectors is integration of sensor and front-end electronics on the same silicon chip.

The presented dissertation study was created to show the current state of research which is represented by the imaging pixels detector X-CHIP-02. Specifically, this study focuses on the development of the pixel detector X-CHIP-02 which is manufactured in ultra-deep submicron 180 nm SOI CMOS technology. Basic parameters and important blocks of the X-CHIP-02, as well as the latest results, are described. Knowledge and experience with pixel detectors were obtained during solving the research project and grants that were solved at the Department of Microelectronics FEE CTU and at the Department of Physics FNSPE CTU in Prague. The proposals of the chip have been developed in cooperation with Advanced Detection Systems of Ionizing Radiation Project at the FNSPE CTU in Prague. All the relevant circuit blocks of pixels detector X-CHIP-02, tests structures and other prototypes of micloelectronics circuits and datectors designed in 180 nm SOI, 180 nm, 150 nm and 65 nm CMOS technology are presented in this dissertation. The main objectives of this work are in the following reflections:

- Design, implementation and electrical measurement of the X-CHIP-02 pixels detector 180 nm SOI CMOS technology. Functionality verification of the X-CHIP-02 with the TEM, $^{60}$Co and X-rays, characterization of the test structure of the X-CHIP-02 during irradiation.
  - Description of individual processes of radiation resistance of developed structures in 180 nm SOI CMOS technology.
- Development of the second prototype of the X-CHIP-02 pixel detector in 180 nm SOI CMOS technology the X-CHIP-03 and LVDS drivers for the communications.

  - Characterization of the LVDS drivers with electrical measurement. Evaluation of the necessary modifications for the next version of the microelectronic structure for the required communication speed.

- Development of the thirds prototype of the X-CHIP-02 pixel detector in 180 nm SOI CMOS technology the LORDS octagonal pixels detector for Low Earth Orbit (LEO) with required parameters of this detector for the purpose of its use LVDS drivers modification for the large - scale detectors. The electrical measurements of the pixel electronics and its radiation tolerance.

  - The verification of the LVDS drivers, Development the detector with Analog to Dicital Converter (ADC) mode and implementing a voltage density improvement in the sensor (handle wafer) by an octagonal sensor design.

- Development, implementation, electrical measurement and radiation tests at 1000 Mrad in the 65 nm CMOS technology the voltage Digital-to-analog converter with the appropriate circuits to perform the radiation tests.

  - The verification of radiation resistance at 1000 Mrad of the microelectronics structures designed in 65 nm CMOS technology from various sources as $^{60}$Co and X-rays. The first and second prototypes characterization during irradiation of the VDAC and definition of the INLs and DNLs according to requirements.

# Chapter 3

# Physics

The nature of our universe has always intrigued man. The exploration of what we are, why we are, and where we are has been objects of considerable effort since the beginning of our existence see Figure 3.1. Today, constructing and exploiting the tools needed to continue this exploration require extensive collaboration efforts in both economic and intellectual terms. The CERN laboratory is a fruit of a successful collaboration in Europe, now housing many different particle accelerators of varying sizes used to explore physics. Other non-European countries have joined CERN and its many physicists as partners to share this quest for new knowledge.

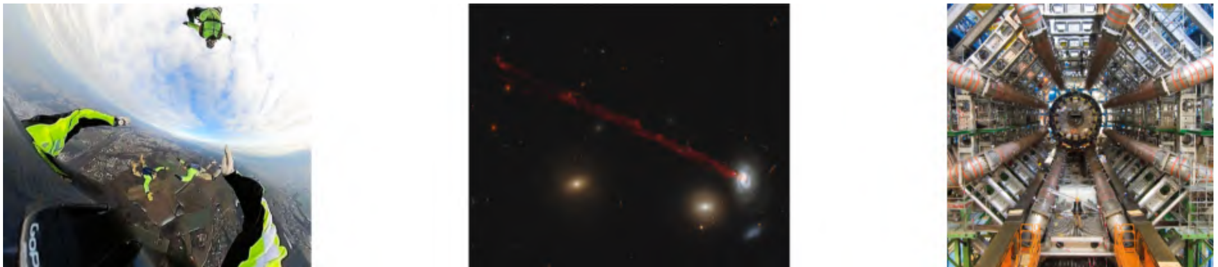

Figure 3.1: In order to explain our everyday world we need two quarks (left). To explain what is happening in our universe we need two more quarks and to explain the formation of our universe [33] as well as certain phenomena we need yet another pair of quarks (middle), for a total of six (right) [34].

Particle accelerators can accelerate different kinds of particles such as electrons, positrons, protons, antiprotons and ions. The accelerated particles are formed into beams which can be guided using magnetic or electrical fields to strike and to interact with the target material or made to collide and interact with other accelerated particles. By studying the results of these interactions our knowledge about matter is successively improved. Increasing the energy of the accelerated particles provides us with a better tool to probe the structure of the particles making up matter and their interactions. An increase of the

particle energy results in an increase of the power of resolution of our observation, which in turn brings us closer to the conditions that existed in our universe at its "birth". This increase in particle energy has a price: either the magnets providing the guiding field are made stronger to contain the particles in the machine or the radius of the accelerator is enlarged [35].

The LHC machine, now being assembled at CERN [36], actually uses both options. The magnetic field used in the main bending dipole magnet is an unprecedented 8.35 T and the circumference of the machine is a huge 27 km. The LHC machine is the last link in a chain of CERN accelerators that are required to permit the acceleration of protons from rest energy to 7 TeV, and important upgrades of all these machines have been made [Ben05] to enable the best possible performance. Many issues related to diagnostics are of vital importance for the technologically very challenging scientific instrument which is the LHC. Particle accelerators are equipped with extensive diagnostic tools and real-time controls. Automatic beam steering, beam tuning and detailed knowledge of the properties of the superconducting magnets, some of the subjects treated in this work, are major issues when trying to reach 7 TeV.

## 3.1 The CERN laboratory

CERN, the European Organization for Nuclear Research, is the world's leading laboratory for particle physics. Its mission is fundamental physics – exploring the fundamental constituents of matter and what the universe is made of. The main tool for research is the Organization's unique network of particle accelerators, which collide beams of particles or direct them to fixed-target experiments. Giant detectors record the results of these collisions, providing data to thousands of physicists from all over the world for analysis.

Founded in 1954, CERN is an intergovernmental organisation headquartered in Meyrin, in the Canton of Geneva, Switzerland (Figure 3.2). It is governed by its 23 Member States. It also brings together eight Associate Member States and six Observers. It has become a prime example of international collaboration, uniting people from all over the world to push the frontiers of science and technology for the benefit of all. The history of CERN is described for example in [35]–[38].

CERN has two main campuses, the original Meyrin site on the French/Swiss border, and the Prévessin site in France. There are also smaller sites around the 27-kilometre ring of the LHC, situated in both countries. These are host to unprecedented experiments resulting from worldwide collaborations between nations, universities, and scientists.

Over 17 900 people from around the world work together on CERN-based projects, constantly advancing the limits of knowledge. Around 3600 of them are employed by

CERN. They take part in the design, construction, and operation of the research infrastructures. CERN staff also contribute to the construction and operation of the experiments, as well as to the analysis of the data gathered for a vast community of users comprising over 12 500 scientists of 110 nationalities from institutes in more than 70 countries [35], [39]. Other personnel consists of associates, fellows, students and contractors.

Figure 3.2: Map of the region close to Geneva where the CERN site is located. The extent of the 27 km Large [40] Hadron Collider is indicated

The Organization's budget for the year 2021 is of the order of 1.347 billion Swiss francs [41]. Contributions are shared between the member states in proportion to their GNP: Germany, Italy, France and the United Kingdom are the main contributors. A number of major non-European nations participate in the LHC accelerator project having an observer status.

In the LHC experiments, ATLAS [2], CMS [3] and ALICE [4] and LHC-b (Figure 3.3), universities and research institutes from all over the world collaborate and contribute to the common effort either with in-kind services and equipment or by sharing costs directly with funds.

ALICE [4], "A Large Ion Collider Experiment", will observe proton and lead ion collisions in LHC. The experiment will study the physics of strongly interacting matter at extreme energy densities, where the formation of a new phase of matter, the quark-gluon plasma, is expected. ATLAS [43], "A Toroidal LHC Apparatus" and CMS, "The Compact Muon Solenoid" [44], look for the Higgs Boson [45], supersymmetry and aspects of heavy ion collisions. LHC-b [46], the LHC Beauty experiment, will make precision measurements of CP violation and rare decays [47].

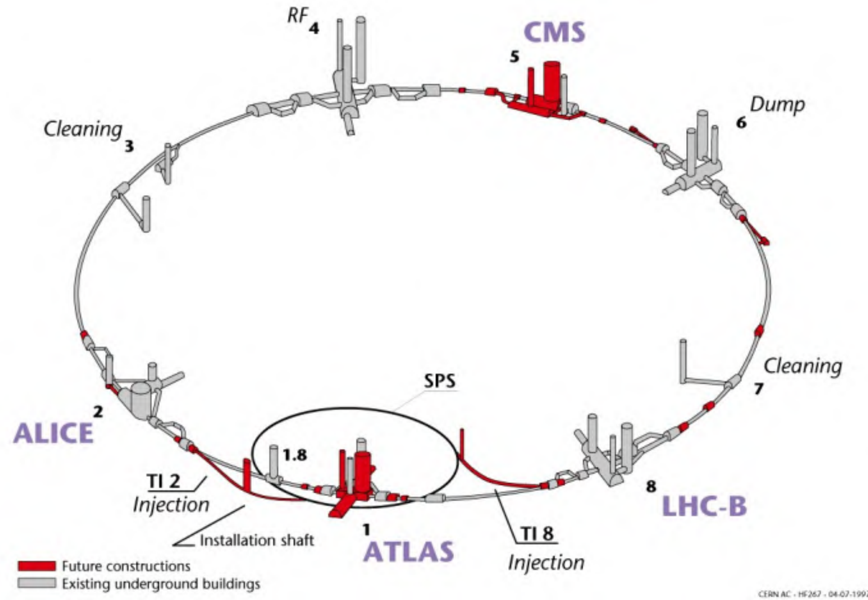


Figure 3.3: The Large Hadron Collider and the experiments Atlas, CMS, LHC-b [42]

### 3.1.1 Background

During the first half of the last century, European achievements and research dominated physics progress. After the Second World War, some of the leading physicists, Rabi, Amaldi, Auger and de Rougemont, realised, that only international co-operation could advance the science of physics and support the construction of new, powerful, expensive research facilities. The creation of a European high energy particle physics laboratory was recommended by a UNESCO meeting in Florence in 1950, and less than three years later a convention was signed by 12 countries creating the Conseil Européen pour la Recherche Nucléaire. Many important ideas and innovations in the accelerator domain have originated at CERN and were developed at machines such as the Intersecting Storage Rings (ISR), the Super Proton Synchrotron (SPS) and the Proton-Antiproton Collider (SppS). The first W and Z particles were produced at SppS , confirming the unified theory of electromagnetic and weak forces. The Large Electron-Positron Collider (LEP) tested extensively, with measurements unsurpassed in quantity and quality, the "Standard Model" [48]. The LEP data are very accurate and have sensitivity to phenomena that occur at energies beyond those of the machine itself, permitting a speculative "preview" of exciting potential new discoveries.

The evidence from LEP data analysis indicates that new physics should be discovered at centre-of-mass energies for proton-proton collisions around 1 TeV.The LHC has been designed for this search and it is now installed in the 27-kilometre tunnel.The LHC will be injected with beams coming from CERN's existing particle sources and accelerators.

This reuse of existing installations has been the hallmark of CERN since its beginning and is one of the major reasons for the laboratory's success and longevity.

The LHC is a superconducting accelerator, by which is understood that the main bending and focussing magnet are built using superconducting technology. The main bending magnet has a field of 8.35 T at 7 TeV proton energy [49]. The LHC will be a versatile accelerator. It will accelerate proton beams to energies around 7 TeV collide them in beam crossing points, providing the experiments with high interaction rates. It will also be able to accelerate and bring into collision beams of heavy ions such as lead with a beam energy of 2.76 TeV/nucleon [50]. Colliding lead ions will yield a total centre-of-mass energy of $2\times208\times2.76$ TeV = 1.15 PeV, about thirty times higher than the centre-of-mass energy available at the Relativistic Heavy Ion Collider Relativistic Heavy Ion Collider (RHIC) at the Brookhaven Laboratory in the US [51].The LHC has been designed for theoretically predicted phenomena; however the machine is also built to offer possibly new discoveries not predicted by current theory [35].

## 3.2 Physics motivation

Physics tries to give unified descriptions of the behaviour of matter and radiation. For a long time physicists considered matter to be constituted by fundamental particles and constructed an elaborate system of particle classification. The present "Standard Model" of particle physics sorts the elementary particles into three families, see Table 3.1. There are two quarks (and their antiparticles) and two leptons in each family: the "up" and "down" quarks, the electron and the electron-neutrino are in the first; the "strange" and the "charm" quark, the muon and the muon neutrino in the second; the "top" and the "bottom" quark, the tau and the tau neutrino in the third [52]. The Standard Model contains both fermionic and bosonic fundamental particles. Fermions are particles which possess half-integer spin and obey the Pauli exclusion principle, which states that no fermions can share the same quantum state. Bosons possess integer spin and do not obey the Pauli exclusion principle. Informally speaking, fermions are particles of matter and bosons are particles that transmit forces [48].

| Generation 1 (ordinary matter) | | | |
|---|---|---|---|
| Fermion (Left -handed) | Symbol | Electric charge | Mas |
| Electron | e | -1 | 0.511 MeV |
| Electron neutrino | $v_e$ | 0 | <50 eV |
| Positron | $e^c$ | +1 | 0.511 MeV |
| Electron antineutrino | $v_e^c$ | 0 | <50 eV |
| Up quark | u | +2/3 | $\sim$5 MeV |
| Down quark | d | -1/3 | $\sim$10 MeV |
| Anti-up antiquark | $u^c$ | -2/3 | $\sim$5 MeV |
| Anti-down antiquark | $d^c$ | +1/3 | $\sim$10 MeV |
| Generation 2 | | | |
| Muon | $\mu$ | 1 | 105.6 MeV |
| Muon neutrino | $v_\mu$ | 0 | <0.5 MeV |
| Anti-Muon | $\mu^c$ | +1 | 105.6 MeV |
| Muon antineutrino | $v_c^\mu$ | 0 | <0.5 MeV |
| Charm quark | c | +2/3 | $\sim$1.5 GeV |
| Strange quark | s | -1/3 | $\sim$100 MeV |
| Anti-charm antiquark | $c^c$ | -2/3 | $\sim$1.5 GeV |
| Anti-strange antiquark | $s^c$ | +1/3 | $\sim$100 MeV |
| Generation 3 | | | |
| Tau lepton | $\tau$ | -1 | 1.784 GeV |
| Tau neutrino | $v_\tau$ | 0 | <70 MeV |
| Anti-Tau | $\tau^c$ | +1 | 1.784 GeV |
| Tau antineutrino | $v_c^\tau$ | 0 | <70 MeV |
| Top quark | t | +2/3 | 173 GeV |
| Bottom quark | b | -1/3 | $\sim$4.7 GeV |
| Anti-top antiquark | $t^c$ | -2/3 | 173 GeV |
| Anti-bottom antiquark | $b^c$ | +1/3 | $\sim$4.7 GeV |

Table 3.1: Fermions: leptons and quarks [35].

In the Standard Model, the theory of the electroweak interaction (which describes the weak and electromagnetic interactions) the forces between fermions are modeled by coupling them to bosons which mediate (or "carry") the forces [53]. The bosons in the "Standard Model" are:

- Photons, which mediate the electromagnetic interaction.
- W and Z bosons, which mediate the weak electromagnetic force (discovered at CERN).
- Eight species of gluons, which mediate the strong nuclear force.
- The Higgs bosons, which are thought to be responsible for the existence of inertial mass [54], [55].

### 3.2.1 Higher and higher energies

How was all this discovered? To be able to observe the constituents of matter, elementary particles can be used as a probe. In general, a structure can only be resolved by a probe, for example electromagnetic radiation, if the wavelength of the probe is small compared to the size of the structure being studied. To reach the dimensions required for elementary particle research wavelengths below $\lambda < 10^{-15}$m are required since the proton size is approximately $0.879\times10^{-15}$ m [56]. The de Broglie wavelength must be

$$\lambda_B = \frac{h}{p} = \frac{hc}{E}, \tag{3.1}$$

where p and E are the momentum and energy of the particle respectively, assuming $E/E_0 \gg 1$, where $E_0$ is the rest energy. To be able to produce new particles we need the energy, according to the fundamental equation

$$E = mc^2 \tag{3.2}$$

Most particles are only produced together with their antiparticles, for example electron and positron pairs are produced by letting high energy gamma-rays strike a target made of heavy nucleus matter. At the collision, the nucleus itself gains some energy (conservation of momentum) and this energy is lost for particle production. Thus the gamma-ray energy needed for particle production is therefore always higher than what is given in the relation 3.2 above and is:

$$E_\gamma > 2m_e c^2 = 1.022\ MeV \tag{3.3}$$

The threshold energy required for the production of electron-positron pairs, where each particle has a mass $m_e = 9.109\ 10^{-31}$kg, corresponds to a rest mass of 511 keV. This explains why the probe used needs higher and higher energies when the substructure of matter has to be explored in depth [35]. The first experiments in particle physics used particles from matter with natural radioactivity (alpha particles and electrons). But it was rapidly realized that higher energies than those provided by natural sources were needed to permit a deeper penetration into the atom's nucleus. The first accelerating devices used electrostatic fields to increase the particle energy [57], [58]. Acceleration of protons was first made using linear accelerator technology at Berkeley [59]. To further increase the available energy for acceleration, the machine builders moved to circular accelerator designs where the particles pass an electrostatic field at each revolution and gain energy as they circulate around the machine in the vacuum chamber. This design required the introduction of magnetic fields perpendicular to the trajectory corresponding to the change of momentum to keep the particles on their circular trajectories. The

principle of "strong focusing" which is important to keep the expensive magnet aperture small was described first by [60]. The principle of the alternating gradient synchrotron was published by Courant et al. [61]. Strong focusing is based on a long-known result in classical optics: combined alternating focusing and defocusing lenses have a net focusing effect. A focusing quadrupole, in one plane, is defocusing in the other. In both planes we thus have a net focusing effect from a chain of alternating focusing and defocusing magnets (alternating-gradient focusing). All the circular accelerators at CERN are today synchrotrons, where both the revolution freauency and the fields vary with the energy of the accelerated particle. The maximum energy that a cyclic accelerator can give to a given particle is typically limited by the available strength of the magnetic bending field and the maximum radius the particle can have in the vacuum chamber. Higher particle energies need higher fields for a given machine radius and superconducting magnets, though complex and requiring elaborate infrastructures, are today used to obtain the required high magnetic fields [35].

In the CERN context the particles are extracted from the particle source, a device generating gas plasma. The particles are then extracted from the source and accelerated in a linear accelerator. The particles, now in the form of a bunched beam, are subsequently injected into a chain of synchrotron machines and accelerated up to the energy defined for any given physics experiments. The beams are made to collide, or alternatively, are extracted for fixed target physics. In the LHC case this staged acceleration means that a particle will have to pass through 5 different machines, each time increasing the energy of the particle as it passes through. In the section 3.3 an overview of the CERN accelerator complex is described.

## 3.3 The CERN particle accelerators

There is a variety of accelerator designs more or less suitable for given particles, energies, intensities, etc. However, to be able to substantially increase the kinetic energy of the particles accelerated, an interconnected chain of accelerators is necessary. Such a chain of machines permit an easier design and the optimization of the range of the different individual accelerator stages. Particles of different types can be accelerated in the machines depending on the experimental needs: electrons, positrons, protons, antiprotons and ions [62]. The particle sources, which provide the particles to be accelerated, can be of many types and at CERN there are proton, ion and electron sources. Particles can also be produced by collecting the debris created by primary beams hitting a target at high energy. In this case the particles created by the collisions are collected after the target station, refocused and accelerated or decelerated in down-stream machines. This is the classical method to create beams of antiprotons or positrons. Protons are produced in a source, a duoplasmatron and injected into the Linac 2 which is a linear accelerator [63]. In the Linac 2 the protons are bunched and accelerated to 50 MeV energy, split into 4 parts and injected into the next machine which has four vertically stacked circular vacuum chambers, the Booster rings (PSB), using a multi-turn injection technique. In the PSB the four proton beams are simultaneously accelerated up to 1.4 GeV, extracted, recombined into a single beam and injected into the Proton Synchrotron (PS). The PS continues the acceleration of this single beam up to 28 GeV at which energy the beam is extracted and sent through a long beam line and injected into the SPS, Figure 3.4. The SPS accelerates the beam up to a nominal energy of 450 GeV and it is either extracted for injection into LHC or into the North Zone for fixed target physics. The first extraction tests of a nominal LHC beam from the SPS into one of the LHC transfer lines, TI8, was successfully done in 2005. The LHC will be able to accelerate both protons and lead ions. The Linac 3 in combination with the Low Energy Ion Ring (LEIR) will create high density ion beams for LHC. LEIR will in this configuration act as an on-line accumulator of the beams coming from the Linac 3 machine. The accumulated beams in LEIR will be cooled by an electron cooler with quasi mono-energetic electrons to align the momentum vectors of the ions and minimize energy dispersion [64]. When sufficiently many ions have been accumulated in LEIR they are extracted and transferred through the PS and the SPS machines to the LHC, where they will be accelerated and brought into collision for physics in the experiments.

The 1984 Nobel price in physics was attributed to Simon van der Meer and Carlo Rubbia for the discovery of the $Z^0$ and the W bosons, communicators of weak interaction [66]. This discovery was made possible by colliding protons and antiprotons in the SppS. Quantities of antiprotons usable for particle physics purpose were accumulated

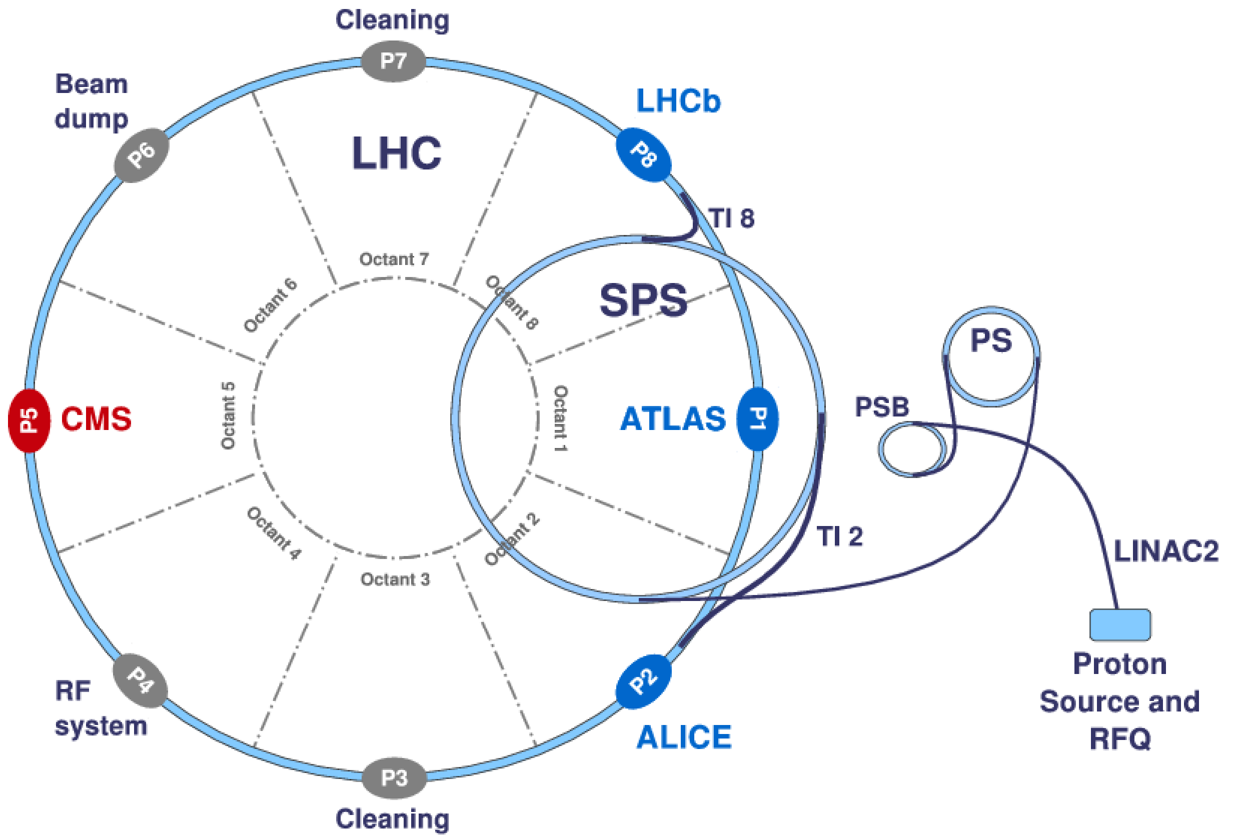


Figure 3.4: The PS and the SPS accelerator complex [65].

in a new machine, the Antiproton Accumulator. To be able to accumulate any appreciable amounts of antiprotons S. van der Meer applied his revolutionary technique, "stochastic beam cooling", which permits precise control of the emittance of the stacked antiproton beam [67], [68]. An additional ring, the Antiproton Collector (AC), was later built around the Antiproton Accumulator (AA) to increase the intensity of the antiproton source by one order of magnitude. In the early nineties, the AA was dismantled and the AC was converted into the Antiproton Decelerator (AD) to serve as a source for antimatter experiments.

# Chapter 4

# Pixel detector in SOI CMOS technology

This chapter describes the pixel detector the X-CHIP-02 designed in 180 nm SOI technology. The section 4.1 described the introduction to theoretical background of the pixel detector design in SOI CMOS technology. The developed design is shown in section 4.2. The essential part of the chapter is in the section 4.3 and section 4.4 where are described the main elements of sensor design. Radiation tests with X-rays and $^{60}$Co are described in section 4.5 and section 4.7. Individual findings, conclusions, and measurements has been made by the author

All parts of this chapter have been published by the author with major contribution in the following reference

- T. Benka, M. Havranek, M. Hejtmanek, *et al.*, "Characterization of pixel sensor designed in 180 nm SOI CMOS technology", *JOURNAL OF INSTRUMENTATION*, vol. 13, 2018, 19th International Workshop on Radiation Imaging Detectors (IWORID), AGH Univ Sci & Technol, Krakow, POLAND, JUL 02-06, 2017, ISSN: 1748-0221. DOI: 10.1088/1748-0221/13/01/C01025

and with a percentage uniform distribution for all the authors mentioned:

- M. Havranek, T. Benka, M. Hejtmanek, *et al.*, "MAPS sensor for radiation imaging designed in 180 nm SOI CMOS technology", *JOURNAL OF INSTRUMENTATION*, vol. 13, 2018, 19th International Workshop on Radiation Imaging Detectors (IWORID), AGH Univ Sci & Technol, Krakow, POLAND, JUL 02-06, 2017, ISSN: 1748-0221. DOI: 10.1088/1748-0221/13/06/C06004
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## 4.1 Background

Silicon is a superior material for sensing visible light, near-infra red light, X-rays, electrons, and many other high-energy charged particles. Furthermore, by using a converting material such as boron or gadolinium, it can also become sensitive to neutrons. Silicon is also a superior material for integrated circuits. Owing to these attractive properties, intelligent monolithic radiation sensors have been desired for a long time in high-energy physics, synchrotron-light source experiments, X-ray astronomical satellite, and many other scientific fields [70].

In high-energy physics experiments, silicon sensors are mainly used to detect short-lived charged particles generated by high-energy beam collisions. At present, they are mainly fabricated as a hybrid detector consisting of a silicon sensor and the readout Large Scale Integration (LSI) bonded via metal bumps [71]. Although hybrid detectors have achieved very good performance in many experiments, they also have several limitations, e.g., the pixel size is limited by the bump size of $\approx 50$ $\mu$m, and the cost of the production of millions of bonding bumps is high.

To catch photons or particles having high penetrating power with high efficiency, a thick depletion region must be formed with high voltage biasing. However, a high-voltage region causes difficulties in integrating transistors in the LSI. When SOI technology emerged, it was considered to provide the ideal structure for monolithic radiation detectors [72]. It provides a thick sensing region in the handle wafer, and CMOS circuits can be fabricated in the top Si layer. Research and development studies on monolithic SOI pixel detectors [70], [73] revealed issues that must be solved.

Radiation damage: SOI devices are robust against the SEE because an active Si is very thin (<40 nm). However, they are not hard against the Total Ionization Dose (TID) effect since SOI has a relatively thick BOX layer under the transistors that accumulates trapped holes generated by radiation. The required radiation hardness differs depending

on the application, but some applications require more than 100 kGy(Si) tolerance, which far exceeds the standard SOI device radiation hardness.

- Back-gate effect: a high voltage (∼100 V) applied to the sensing region induces back-side channel formation in transistors. This causes a shift in the threshold voltage and drain current leakage.
- Coupling between sensors and circuits: sensors and circuits are located near each other, separated by a buried oxide (BOX) layer of about 200 nm thickness. This causes cross talks, signal oscillation, and increased noise level.
- Radiation damage: SOI devices are robust against the SEE because an active Si is very thin (<40 nm). However, they are not hard against the TID effect since SOI has a relatively thick BOX layer under the transistors that accumulates trapped holes generated by radiation. The required radiation hardness differs depending on the application, but some applications require more than 100 kGy(Si) tolerance, which far exceeds the standard SOI device radiation hardness.

Owing to these issues and the ease of accessing technologies, many research and development studies of monolithic sensors are being carried out using commercial CMOS technologies [19], [23] Usually, the epitaxial layer is used as the sensing region, but the thickness of the epitaxial layer is less than 30 $\mu$m and it is very difficult to form a thick depletion region using a conventional CMOS technology. An approach using a high-voltage CMOS process is also being pursued, but the circuit integration level is very limited [74]. To solve these issues, we have developed an SOI pixel process based on the 0.18 $\mu$m SOI CMOS process. Figure 4.5 and 4.4 show a cross-section view of the SOI pixel detector. To achieve a thick depletion region with an easy-to-operate voltage, we fabricated SOI wafers bonded with a high-resistivity floating-zone (FZ) handle wafer using Smart Cut technology [75], [76], which can bond two different kinds of Si wafer [70].

The BOX layer isolates the CMOS electronics implemented on a thin, low resistivity, epitaxial silicon layer from a thick, high resistivity handle wafer. The sensitive element, reverse biased PN junction, is integrated in the handle wafer as illustrated in Figure 4.6. In contrast to other SOI technologies, the thick film SOI provides a double well structure to shield the thin gate transistors from the BOX layer. The solution makes this technology a promising option for radiation imaging. The TID and absence of back gate effects were proved by measurement of real structures irradiated up to 700 Mrad [77]. The electrical parameters of CMOS electronics components degrade with accumulated TID due to radiation damage. The modification of the electrical parameters is caused by the sum of two contributions. The first one creates the positive charge trapped in the gate

oxide and the Shallow Trench Isolation (STI). The second one produces the Si-$SiO_2$ interface traps, as shown in Figure 4.6. The biggest difference between the radiation response of MOS transistors fabricated on bulk silicon and transistors in SOI technology is the BOX layer inclusion, which makes SOI transistors more sensitive to TID damage. This is mainly caused by trapped charge in the BOX layer [78], [79], which can affect the threshold voltage of MOSFETs. Characterization of the radiation resistance (TID effect) of the SOI CMOS technology is given by K. O. Petrosyants in [15] and H. J Barnaby in [80]. The chosen technological process allows to apply high bias voltages (up to 200 V), which are used to partially deplete the substrate and to fabricate devices with higher resistivity. Therefore, a fully depleted structure could be realized after substrate thinning. At this time, there is no backside processing. Thus, the HV is applied from the top side using an ohmic contact. The pixel electronics is processed on a 3.5 $\mu$m thin epitaxial layer separated from the handle wafer by a 1 $\mu$m thin BOX layer. The electronics circuit of each pixel is located in insulated substrate which is surrounded by Deep Trench Insulation (DTI) in detail is descibed in [19] by the author.

## 4.2 Developed design

The X-CHIP-02 was developed with the Center of Applied Physics and Advanced Detection Systems (CAPADS) at the FNSPE CTU in Prague whose main task is development a new type of X-ray imaging detector using a 180 nm deep submicron Silicon On Insulator (SOI) CMOS commercial technology and its layout is shown in Figure 4.2. The X-CHIP-02 is a special class of MAPS. The first prototype fabricated, the X-CHIP-02, is 300 $\mu$m thick and backgriding from original is 745 $\mu$m, with a size 3.125×3.2 $mm^2$. Two pixel matrices are integrated in the chip. They differ by pixel pitch which is 50 $\mu$m and 100 $\mu$m. Each pixel contains sensitive diode and front-end electronics for signal amplification and hit-counting. More detailed description of the pixel is show in the following sections by the author in [19]. The detailed photo of the X-CHIP-02 an one pixel structure without electronics the 100 $\mu$m pixel is shown in the Figure 4.3. On the right side is the photo of the pixels test structure (measurement capacitance of the sensor) and the clear ribbing is the DTI layer.

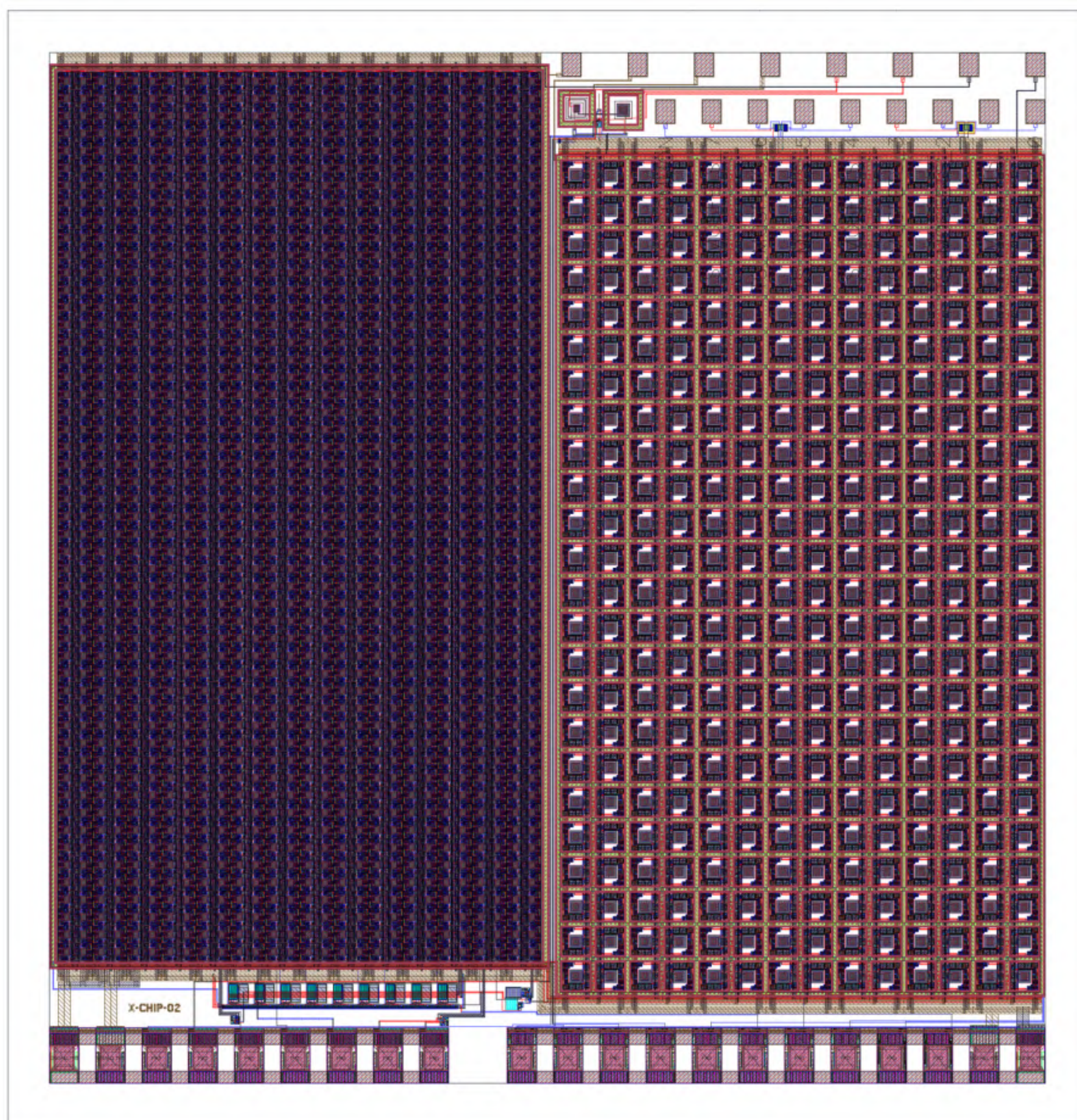



Figure 4.1: The layout of X-CHIP-02.

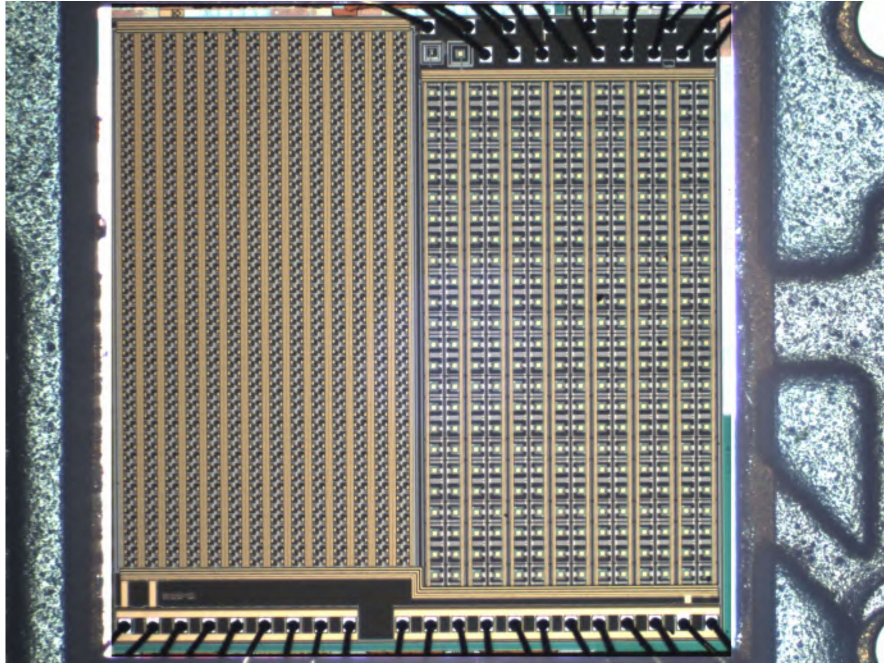
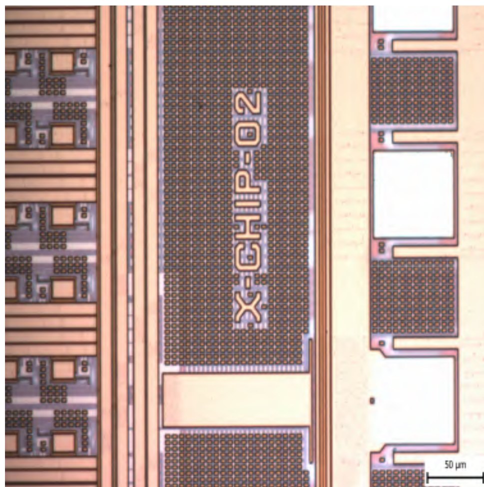


Figure 4.2: The X-CHIP-02 wirebonded on the PCB. On the left side of the chip there is 50 $\mu$m pixel pitch matrix with dimensions 2.55×1.4 mm$^2$ and on the right side there is 100 $\mu$m pixel pitch matrix with dimensions 2.44×1.4 mm$^2$.



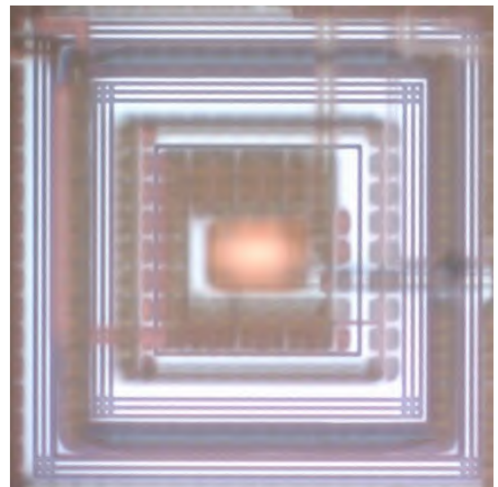



Figure 4.3: (Left) The X-CHIP-02 detailed photography. Small objects are fillers to fill the minimum area of the layers. On the right is an open passivation for the wire bonding. The coarse wires crossing the chip represent the power supply in the top metallization. (Right) Detail of the 100 $\mu$m pixel (test structure without electronics focused on DTI) [19].

## 4.3 Layout of sensitive elements

The electronics is processed on a 3.5 $\mu$m thin epitaxial layer separated from the handling wafer by 1 $\mu$m thin BOX layer. Two different pixel matrices are integrated in the chip. Layout of 50 $\mu$m pixel is shown in Figure 4.4. The sensitive PN junction is formed by P-TYPE handle wafer and the N-Buried Handle Wafer Diode Module (NBUR). When high negative voltage is applied to the handle wafer a depletion region forms around the PN junction. Thickness of the sensitive depleted layer is expected to be approximately 30 $\mu$m at negative bias voltage of 100 V. The handling-wafer is biased by bias ring around entire matrix of 50 $\mu$m pixels. The NBUR layer is biased through a forward biased diode formed by P+ region in the N-WELL. DIODE_BIAS voltage should be slightly positive (1.8 V). The sensor diode is AC coupled to the Charge Sensitive Amplifier (CSA).

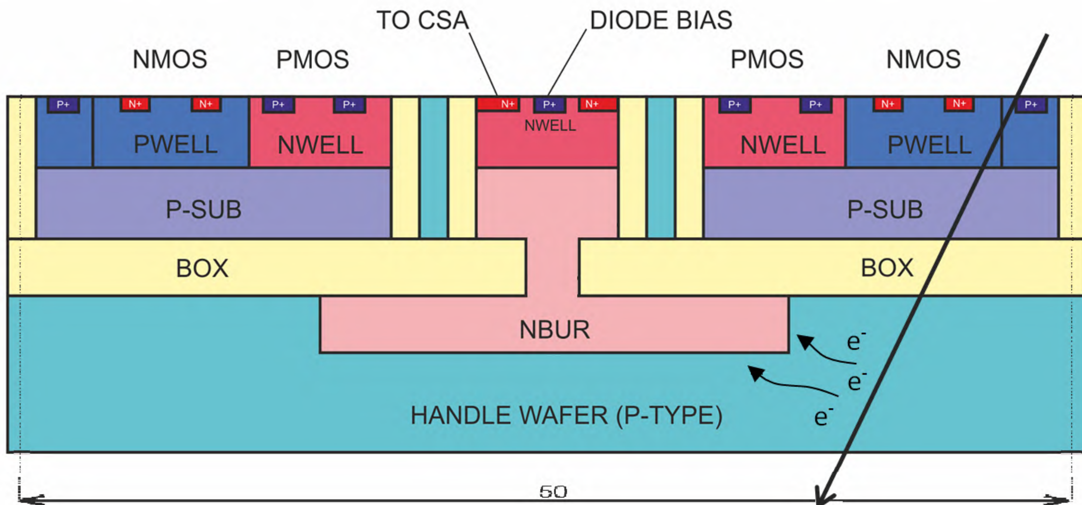



Figure 4.4: Layout of the 50 $\mu$m pixel. All dimensions are in $\mu$m. NMOS and PMOS transistors are just for illustration.

The deep NBUR layer is connected to the readout circuitry (TO_CSA, DIODE_BIAS) as illustrated in the pixel cross section shown in Figure 4.4 and 4.5. The Difference between 100 $\mu$m and 50 $\mu$m pixels is the overall pixel size and the size of charge collecting NBUR implant. The second major difference is following: each pixel has its own implant to bias the handle wafer which might be beneficial to achieve homogenous biasing of the pixel matrix (this implant was not possible to integrate to 50 $\mu$m pixels due to pixel area contains).

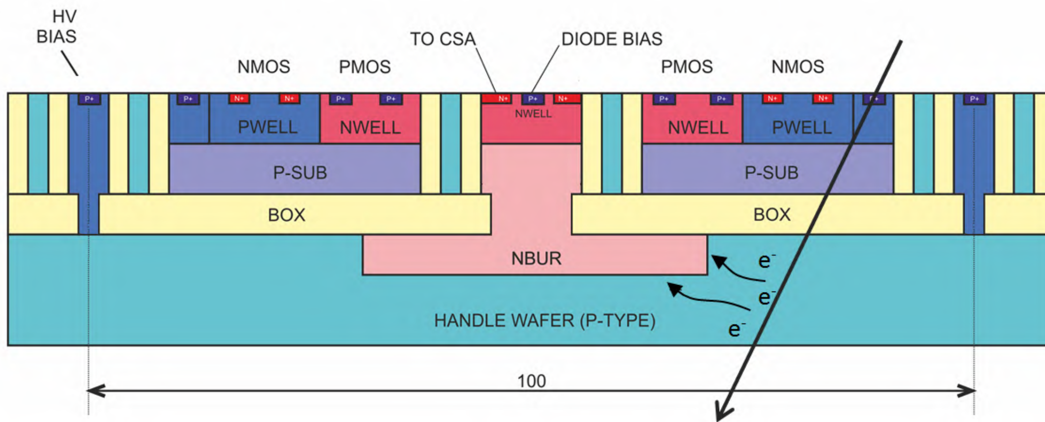



Figure 4.5: Layout of the 100 $\mu$m pixel. All dimensions are in $\mu$m. NMOS and PMOS transistors are just for illustration.

## 4.4 Pixel electronics

The communication with a pixel of the chip is not possible without the necessary electronics. Each pixel contains sensitive diode and front-end electronics for signal amplification and hit-counting. Both pixel types (50 $\mu$m and 100 $\mu$m) have identical pixel electronics. The pixel electronics CSA, discriminator, Digital to Analog Converter for Threshlod adjustment (TDAC), digital logic for configuration and hit counting (Figure 4.6, pixel electronics architecture and layout).

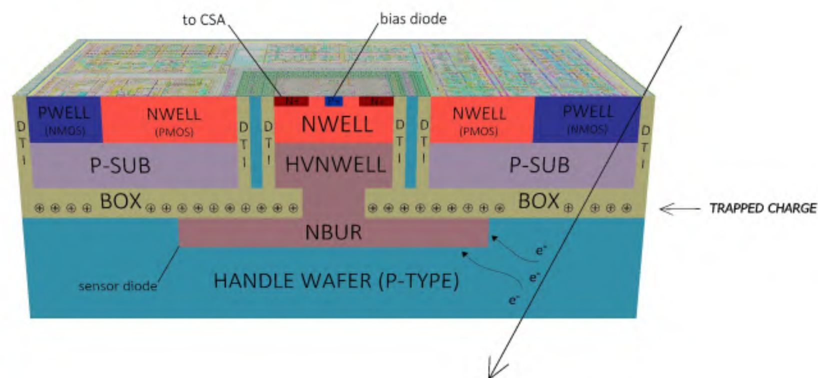



Figure 4.6: Cross section and charge collection of X-CHIP-02. The charge collection in BOX layer arises during irradiation. A high irradiation dose generates the inverse layer of charge in the Handle wafer (SiO–$SiO_2$ interface) [19]. The result is a conductive channel. Avoiding this effect can be accomplished with technology process P-STOP or P-SPRAY, as is described in [81].

Block schematic of one pixel is shown in Figure 4.7 and its layout is shown in Figures 4.8 and Figure 4.9 which comprise these blocks: 1 – TDAC, 2 – discriminator, 3 – CSA, 4 – digital logic, 5 – sensitive and bias diode. Each block and its parameters are described in more detail in subsections below.

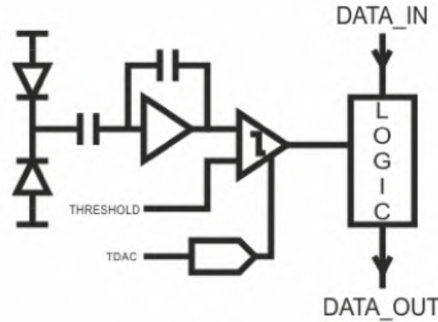



Figure 4.7: Block schematic of pixel circuitry of signal processing.

The difference between pixel matrices is the size of the charge collecting NBUR implant and sensor HV bias connection. The NBUR, along with P-TYPE handle wafer forms the PN junction, which corresponds to the sensor diode. The HV bias ring of the 100 $\mu$m pixel matrix is located in each pixel, but the 50 $\mu$m pixel matrix has only one bias ring around the matrix [82], [83]. Detailed description of the design and communication (digital logic and blocks of the pixel) of the X-CHIP-02 is included in the paper submitted by M. Havranek, T. Benka et al. [25].

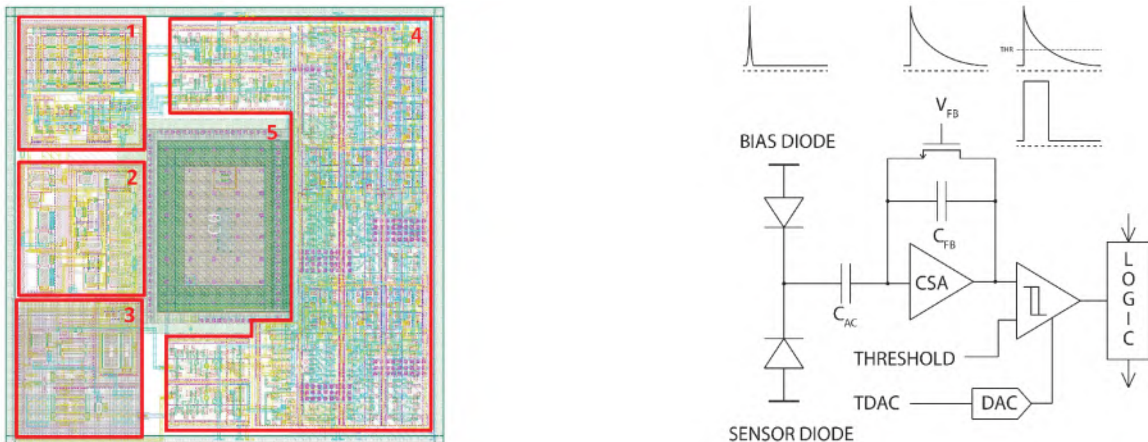



Figure 4.8: The X-CHIP-02 pixel electronics. (Left) The 50 $\mu$m pixel layout: 1 — TDAC, 2 — discriminator, 3 — CSA, 4 — digital logic, 5 — sensitive and bias diode. (Right) Schematic of the integration pixel [19].

The X-CHIP-02 requires a specific interface for data transfer. This is accomplished by a special module between the PC and the chip, the X-CHIP-02-PCB. The setup for

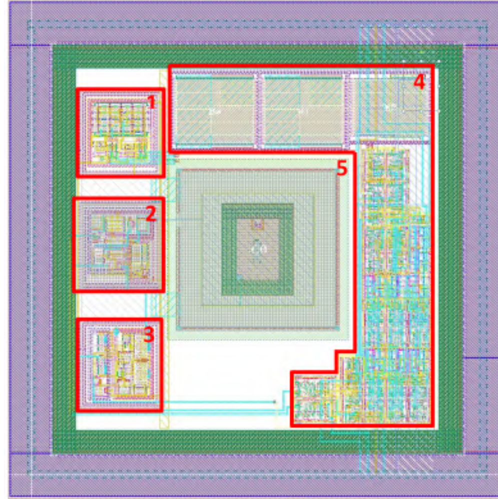



Figure 4.9: The 100 $\mu$m pixel layout, 1 – TDAC, 2 – discriminator, 3 – CSA, 4 – digital logic [19].

the measurement is based on a Simple USB Read-out Equipment (SURE) 4.11) - motherboard, extended by an interface card (X-CHIP-02-PCB - daughterboard, Figure 4.12) with digital IO capabilities and analog blocks (power supplies, voltage and current sources, inject circuit, auxiliary circuits for capacitance measurement of the sensor etc.). An bias currents and voltages are generated on the SURE except for the sensor bias, which can be applied externally [19]. Individual functionalities included in the X-CHIP-02-PCB are enabled by the RC filters for High Voltage (HV) power supply up to 200 V (sensitive diode), for low power supply up to 10 V (bias diode), inject circuit with 2 switch options and the circuit for capacitance measurement of the sensor. The Operational Amplifier (OA) as an integrator with a specific time constant for CLK = 1 MHz, as is shown in Figure 4.10 [19].

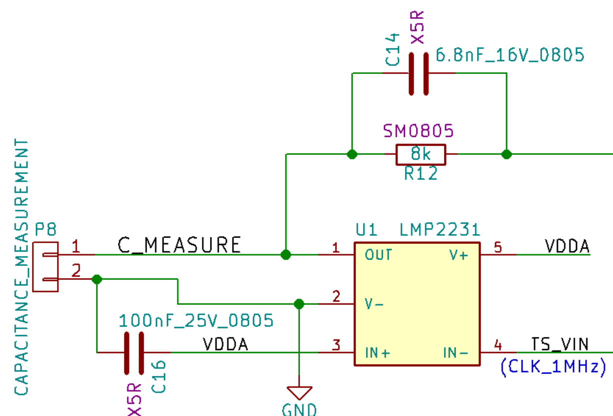



Figure 4.10: Circuit for measurement of capacitance of the sensor.

Figure 4.11: The SURE (motherboard) [19].

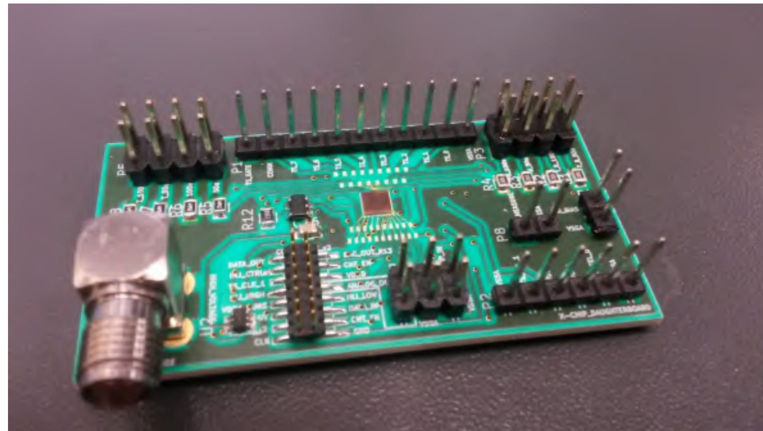


Figure 4.12: The X-CHIP-02-PCB (daughterboard). The X-CHIP-02 is in the middle of the PCB [19].

### 4.4.1 Charge sensitive amplifier

The CSA constitutes the fundamental first stage of most of the front-end electronics for ionizing radiation a particle detector. The CSA converts signal charge sensor diode to voltage and it is the most critical part of the chip. A detailed schematic is shown in Figure 4.13. The layout of CSA is shown in Figure 4.14.

The CSA is AC coupled to the sensor diode which is has two advantages. The first is that the leakage current of the diode does not saturate the CSA and the second involves that the diode can be biased with broader range of voltages without breaking gate of the input transistor of the CSA. The coupling capacitance has been chosen to be as large as possible and at the same time has to fit to the pixel layout. Feedback and injection capacitors have the same value. However, since the feedback capacitance is very small it does not fully determine the closed loop gain of the CSA. In order to determine the closed loop gain of the CSA, a simulation with extracted parasitic capacitances has to be

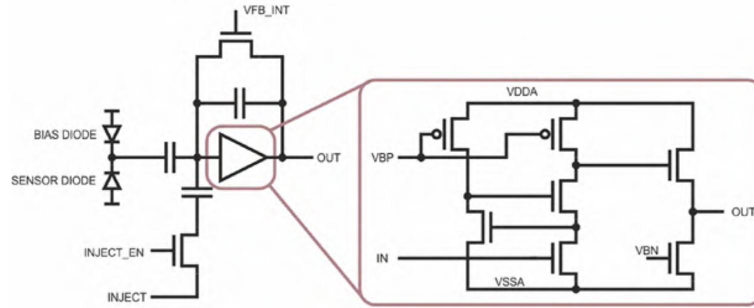



Figure 4.13: Schematic ofthe CSA.

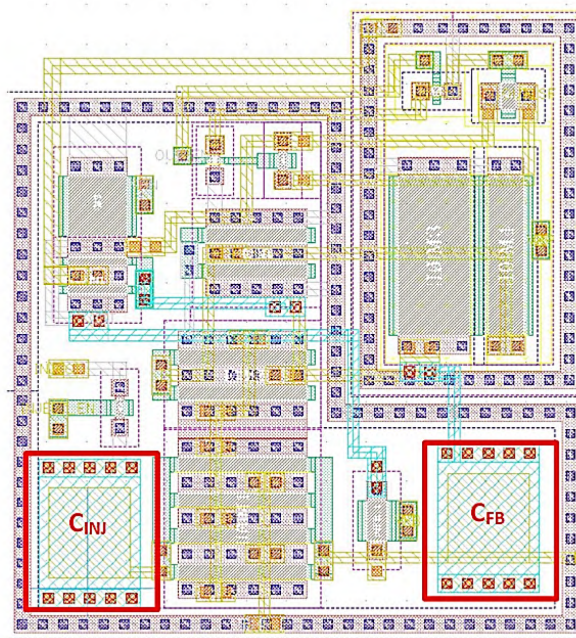



Figure 4.14: Layout of the CSA with $C_{INJ}$ and $C_{FB}$.

done. Important parameters are following: power is 1.37 $\mu$W and open loop gain is 3311. The parameters depend dramatically on bias setting, amplitude of the signal charge and input capacitance.

### 4.4.2 Discriminator with threshold DAC

The discriminator has been designed specifically for the CSA. Low power and compact layout dimensions (14.4×15.9 $\mu$m) have been chosen to fit inside the pixel with pixel pitch of 50 $\mu$m. Special features of the discriminator are tunable hysteresis and 4-bit TDAC which is important to maintain uniform detection threshold in large pixel matrix. The discriminator is implemented by an input differential amplifying stage followed by common source stage and output invertor. In Figure 4.15, the hysteresis is implemented by an extra diff-amp (transistors M11 and M12), which disbalances currents in the input differential

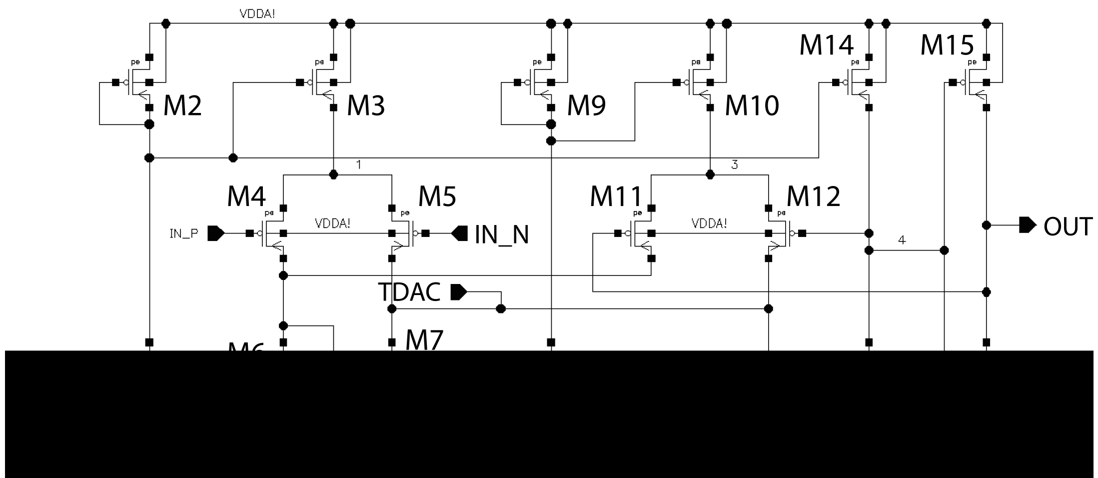



Figure 4.15: The discriminator with hysteresis and threshold schema.

pair of the discriminator (M4 and M5), and thus introducing the hysteresis. This concept was greatly inspired by P. Furth in [84].

An external adjustment of the discriminator threshold is provided by 4-bit current steering CSA. The DAC supplies extra current to one branch of the input differential pair of the discriminator adjusting its effective threshold. The hysteresis is adjustable by a current source in the linear range from -20 mV to 20 mV. The discriminator operates with threshold in the range from -200 mV to 1.23 V while input offset in this range does not exceed 7.5 mV. Layout of the discriminator is shown in Figure 4.16.

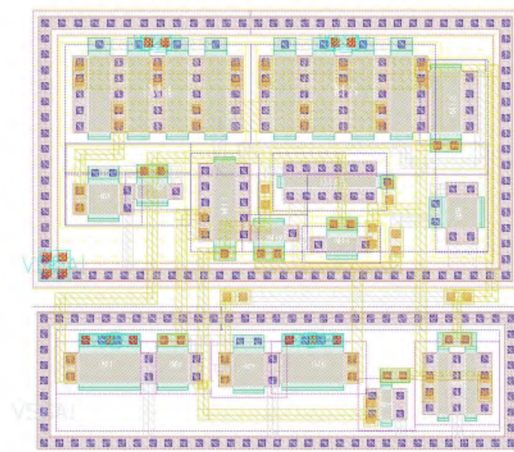


Figure 4.16: The discriminator with hysteresis and threshold layout.

### 4.4.3 Digital logic

Exchange of the data with X-CHIP-02 is done by shift register. Data are loaded and shifted on a rising edge of clock signal. The register includes three sections which are daisy-chained, as shown in Figure 4.17. The sections are following:

- Global configuration register (72 bits)
- 50 $\mu$m pixel matrix (11424 bits)
- 100 $\mu$m pixel matrix (2688 bits)

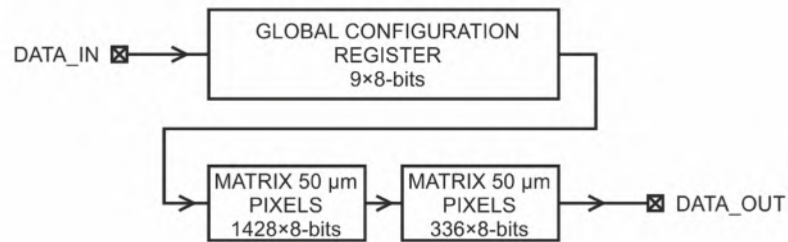



Figure 4.17: The structure of shift register in X-CHIP-02.

The first part of the shift register is the Global configuration register with 72 bits length. Purpose of the global configuration register is solely for configuration of global DACs. The register contains 72 bits. The global DACs have 8-bit resolution and provide 9 voltages from 0 to 1.8 V (8×9). The next part is the 50 $\mu$m pixel matrix which has size of 28×51 pixels (11424 bits). All pixels are identical and each pixel has 8-bit configuration register. Structure of the register and its geometrical orientation are shown in Figure 4.18. The orientation of the matrix corresponds to orientation of the chip as is shown in Figure 4.1. The third part is the 100 $\mu$m pixel matrix which has the same configuration as the 50 $\mu$m pixel matrix. The only difference are matrix size of 14×24 pixels (2688), as is shown in Figure 4.18.

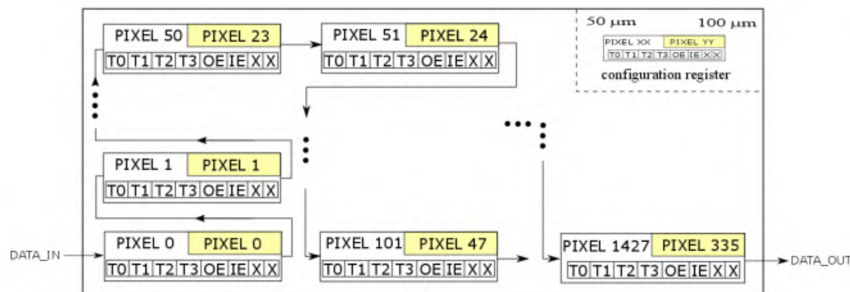



Figure 4.18: The structure of 50 $\mu$m and 100 $\mu$m pixel matrix.

## 4.5 Test structures

The X-CHIP-02 design contains a number of test structures which are useful for a better characterization of individual blocks. They are described in following sections.

- Amplifier
- Transistors for radiation test
- Circuit for precise determination of sensor capacitance

### 4.5.1 Amplifier

The first test structure is an amplifier connected as an unity gain buffer. Input and output of the amplifier are connected directly to the IO pads of the chip, as shown in Figure 4.19.

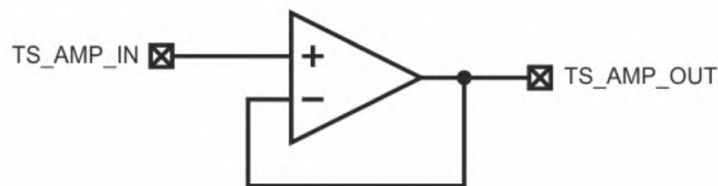



Figure 4.19: The schematic of stand-alone amplifier.

The rail to rail analog buffer depicted in Figure 4.20 consists of two wide-swing differential amplifiers, layout Figure 4.21. A method for extending the input voltage swing of the buffer is using two complementary diff-amp stages operating in parallel, as described in [85]. The optimized circuit of the analog buffer is intended for monitoring of the output signal from the charge sensitive amplifier and driving capacitive load outside the front-end chip. An important design criterion is fast response of the buffer to the rapid rising edge of the signal coming from the charge sensitive amplifier. Simulated rise-time of the output signal of the buffer is 77 ns with capacitive load of 10 pF and peak to peak voltage 459.1 mV. Falling time is not critical parameter of this design because discharge time of the charge sensitive amplifier is in order of microseconds. The analog buffer is designed to drive capacitance as large as 15 pF which corresponds to common oscilloscope probes.

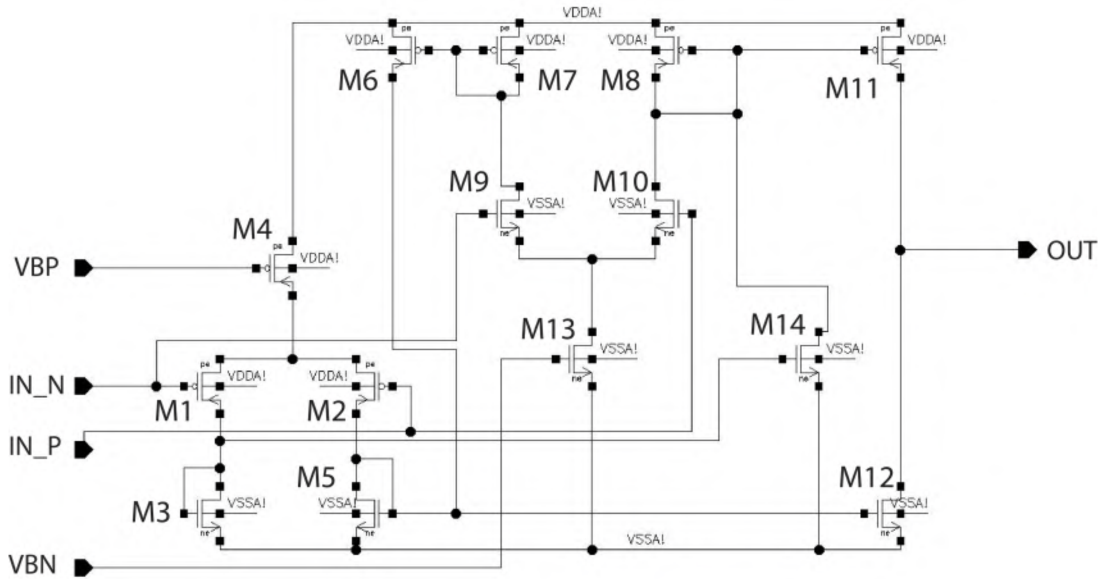



Figure 4.20: The schematic of the rail to rail analog buffer.

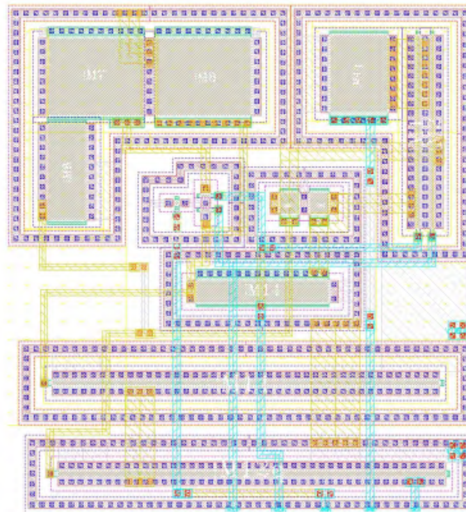


Figure 4.21: The rail to rail analog buffer layout.

### 4.5.2 Transistors for radiation tests

Eight different transistors have been integrated in the chip to assess their radiation tolerance. The transistors are involved in accordance with Figure 4.22 and they have parameters according to the Table 4.1. The transistors structure with the high-voltage p-well High-Voltage P-well (HVP) is shown in Figure 4.23. Threshold shifts of the PMOS and the NMOS transistors before/after exposure to 100 Mrad of $^{60}$Co irradiation for the 180 nm submicron CMOS SOI technology with a few nanometers thick gate oxide are shown in Figure 4.24 and Figure 4.25. The $^{60}$Co irradiation source has the dose of rate of up to 51 krad/min. Annealing of the chip has been at the room temperature. Detailed study of the Transistors the comparative study of the TID radiation effects on

ASICs manufactured in 180 nm commercial technologies is described by M. Marcisovska, T. Benka et al. in [69].

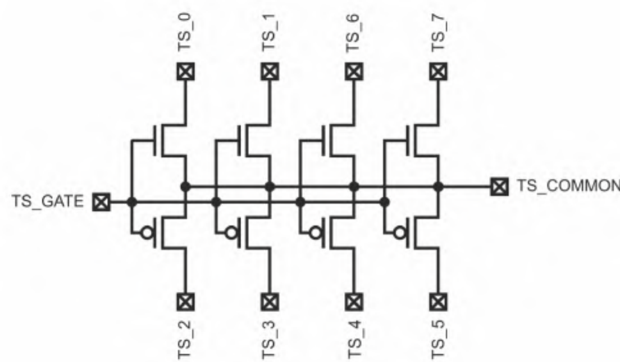



Figure 4.22: The schematic of transistor for radiation tests.

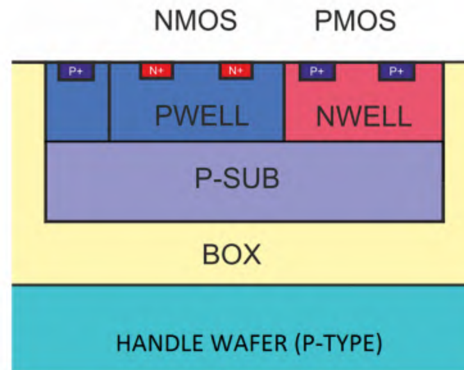



Figure 4.23: The layout of the transistor structures with HVP.

Usage of the HVP might be useful to mitigate the radiation induced back-gate effect. On the other hand, during implantation of the HVP, the surface of the transistors might be significantly damaged leading to various parasitic effects like excessive leakage current or early mobility saturation. The purpose of these test structures is to determine whether it makes sense to use HVP to enhance radiation tolerance and if so, what is its impact on transistor IV characteristics.

| TS | Dimensions (WxL) | TYPE | HVP |
|---|---|---|---|
| 1 | 17.35 $\mu$m $\times$ 8 / 360 nm | NMOS | YES |
| 2 | 2 $\mu$m / 12 $\mu$m | NMOS | YES |
| 3 | 17.35 $\mu$m $\times$ 8 / 360 nm | PMOS | YES |
| 4 | 2 $\mu$m / 12 $\mu$m | PMOS | YES |
| 5 | 17.35 $\mu$m $\times$ 8 / 360 nm | PMOS | NO |
| 6 | 2 $\mu$m / 12 $\mu$m | PMOS | NO |
| 7 | 17.35 $\mu$m $\times$ 8 / 360 nm | NMOS | NO |
| 8 | 2 $\mu$m / 12 $\mu$m | NMOS | NO |

Table 4.1: Description of MOSFET test structures.

For NMOS devices the threshold voltage shifts to more negative values as expected from positive charge build up in the oxide. The slight upturn above 11 Mrad in the NMOS curve is typical and reflects the build up of interface states [78], [86]. About 60 % of the threshold shifts occur during the first 2 Mrad, also a typical phenomenon. Measurements to 100 Mrad on a similar process show a total threshold shift of 25 mV for NMOS with little increase beyond 11 Mrad. Difference between transistors with and without HVP is up to 40 mV. The NMOS transistor structure TS1 has not been functional during the irradiation test.

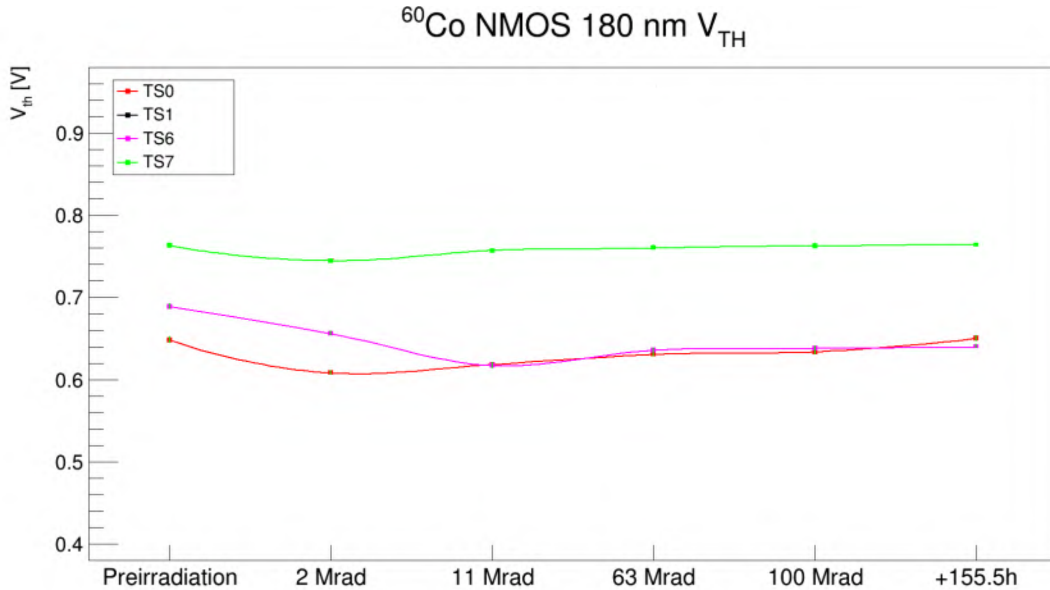



Figure 4.24: Threshold voltage shifts of the NMOS transistors without / with HVP vs. $^{60}$Co radiation dose.

The PMOS structures are a little different then the NMOS structures. Threshold of transistors with HVP is greater by 30 mV than without the HVP. An increase of 100 mV (about 11 Mrad) is resulting from design of PMOS transistor, in detail this issue is solved in [79].

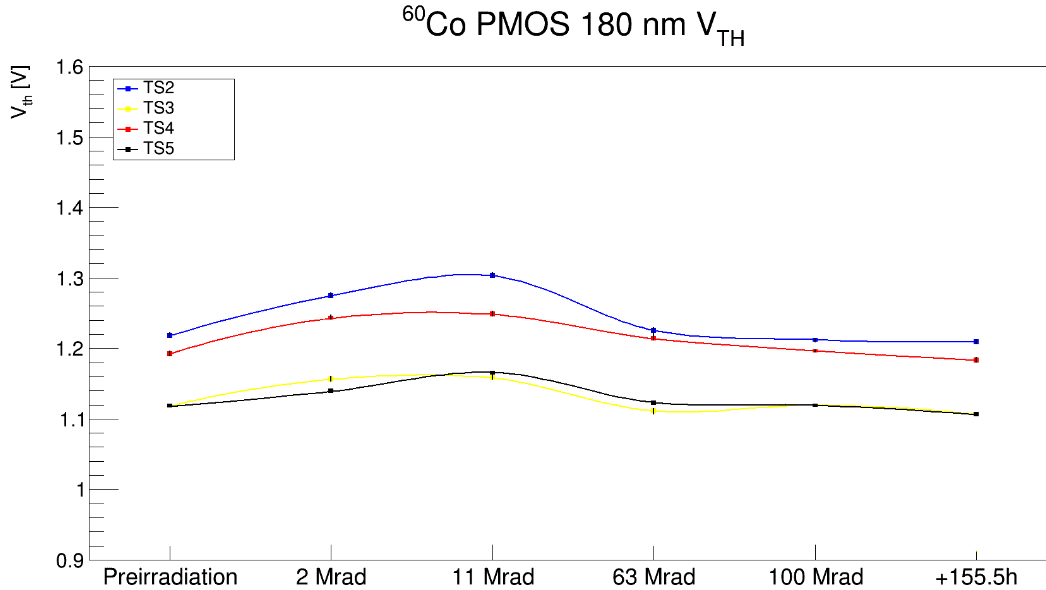



Figure 4.25: Threshold voltage shifts of the PMOS transistors without / with HVP vs. $^{60}$Co radiation dose.

A bit smaller post-radiation degradation is observed in the NMOS transistors T0 and T6 without the HVP. Although the observed degradation is rather small in some cases, typically it is fairly substantial and would need to be compensated for by a considerably higher operating current. The NMOS and PMOS transistors IV-characteristics are shown in following Figures: 4.27, 4.28, 4.29, 4.30, 4.31, 4.32 and 4.33. The beginning of PMOS characteristic is not zero due to measurement error.

A significant effect of radiation damage is shown on Figure 4.26, where is an analog and digital current of the chip. Preirradiation values of the currents have been following: $I_{digital} \approx 400\ \mu$A, $I_{ANALOG} \approx 4$ mA. After 2 Mrad (51 krad/min) the digital current is increased up to 100 mA – 250 times higher. The individual sections of stairs of the currents are due to measurement method. Low levels of the stairs contain the first measurement which measures only transistor structures and the second (high levels) tests the digital communications of the chip. The radiation dose is measured during a temporary interruption of the $^{60}$Co source.

Generally speaking, both bulk and deep submicron SOI CMOS technology is subject to the effects described above.The SOI is often cited as a specifically radiation-hard technology because of its resistance to transient radiation effects, primarily latchup due to photocurrents developed at high intensity bursts of radiation ($> 1{\times}106 - 5{\times}108$ rad), typical for nuclear detonations. Although SOI can provide superior device speed because of reduced stray capacitance, this technology is not inherently more resistant to radiation in our applications. If anything, the additional oxide interfaces tend to complicate matters and at this time most radiation-resistant CMOS processes are on bulk silicon. The most

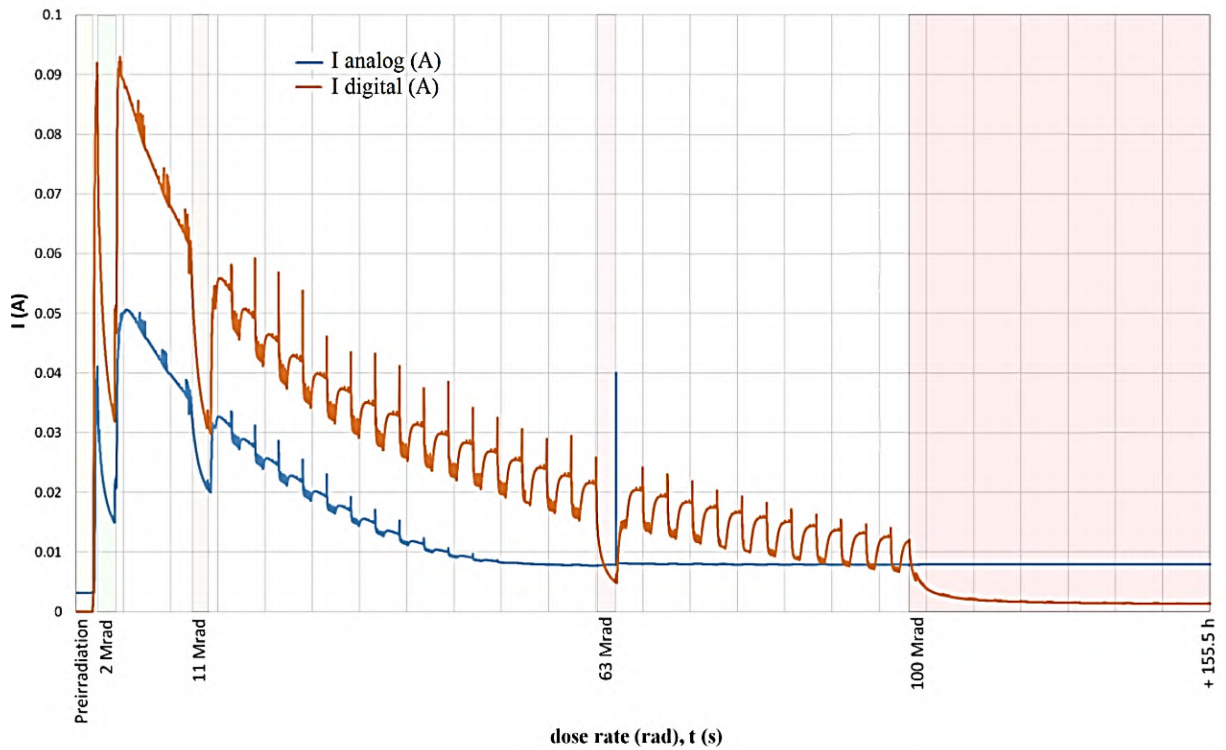



Figure 4.26: (Left) the preirradiation area. The analog and digital current of the X-CHIP-02 during irradiation with $^{60}$Co. (Right) is the afteriradiation region at 155.5 h.

radiation tolerant are mainly submicron CMOS technologies, which are less than 180 nm. Resistance depends on the thickness of gate oxid – bulk damage.

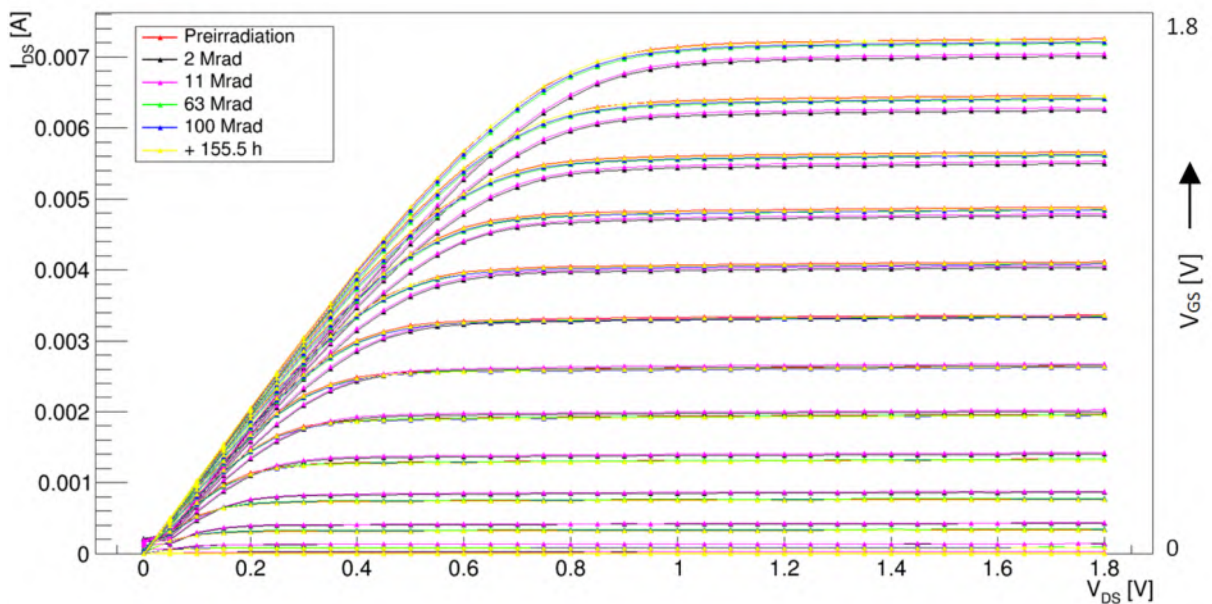



Figure 4.27: IV characteristic of TS0 NMOS with HVP structure in 180 nm CMOS technology for $^{60}$Co radiation dose.

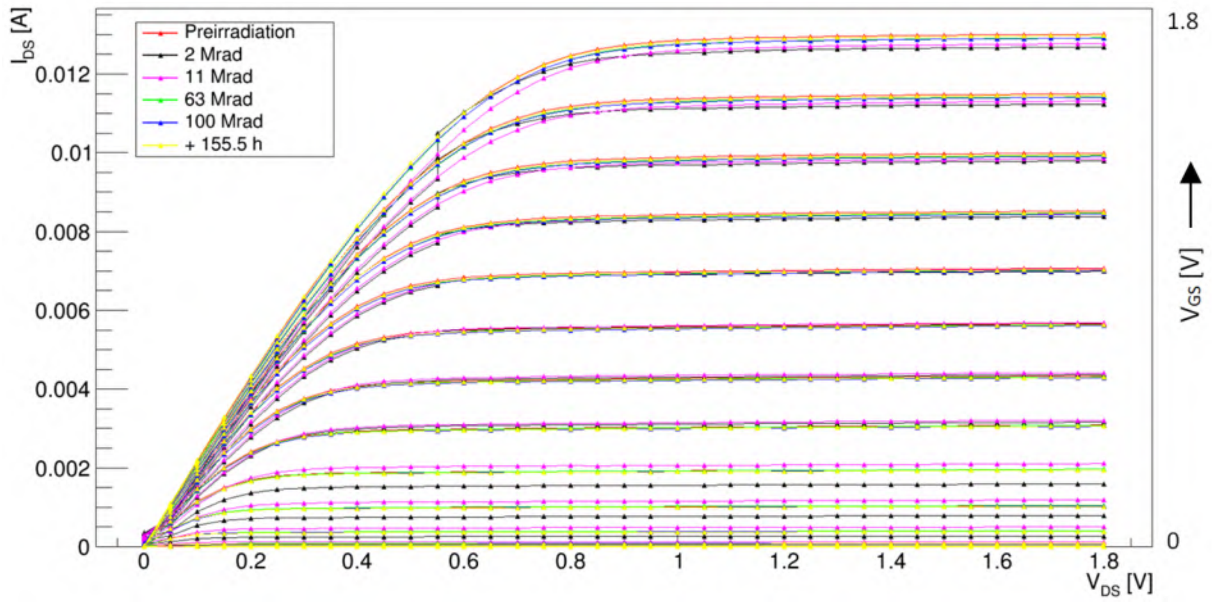



Figure 4.28: IV characteristic of TS6 NMOS without HVP structure in 180 nm CMOS technology for $^{60}$Co radiation dose.

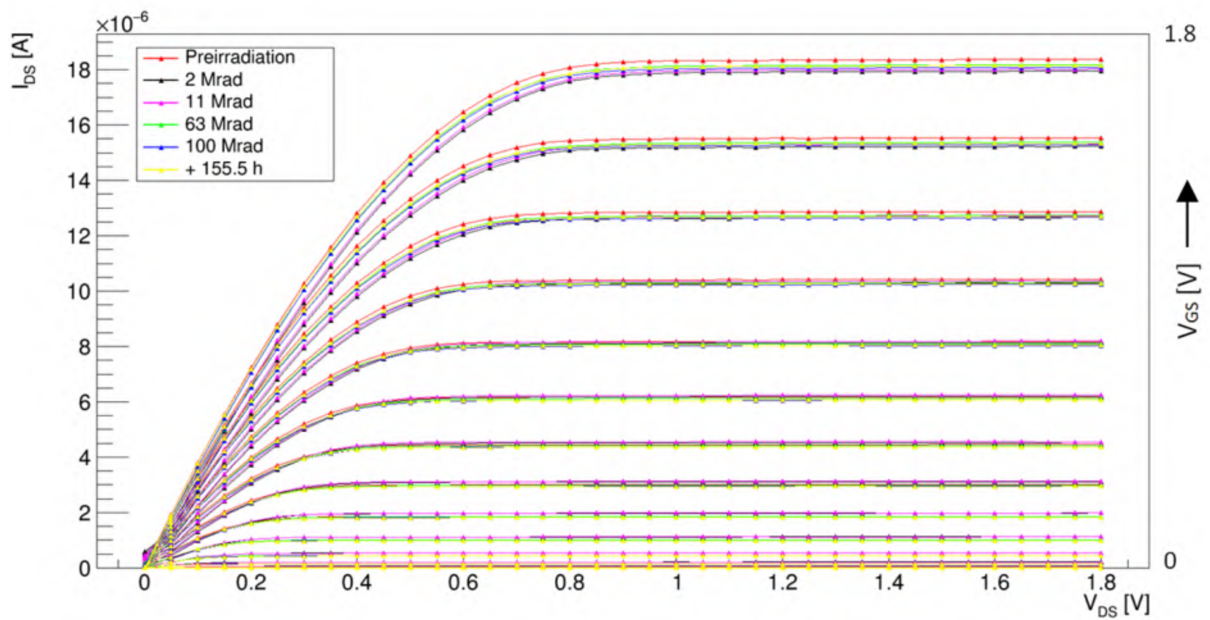



Figure 4.29: IV characteristic of TS7 NMOS without HVP structure in 180 nm CMOS technology for $^{60}$Co radiation dose.

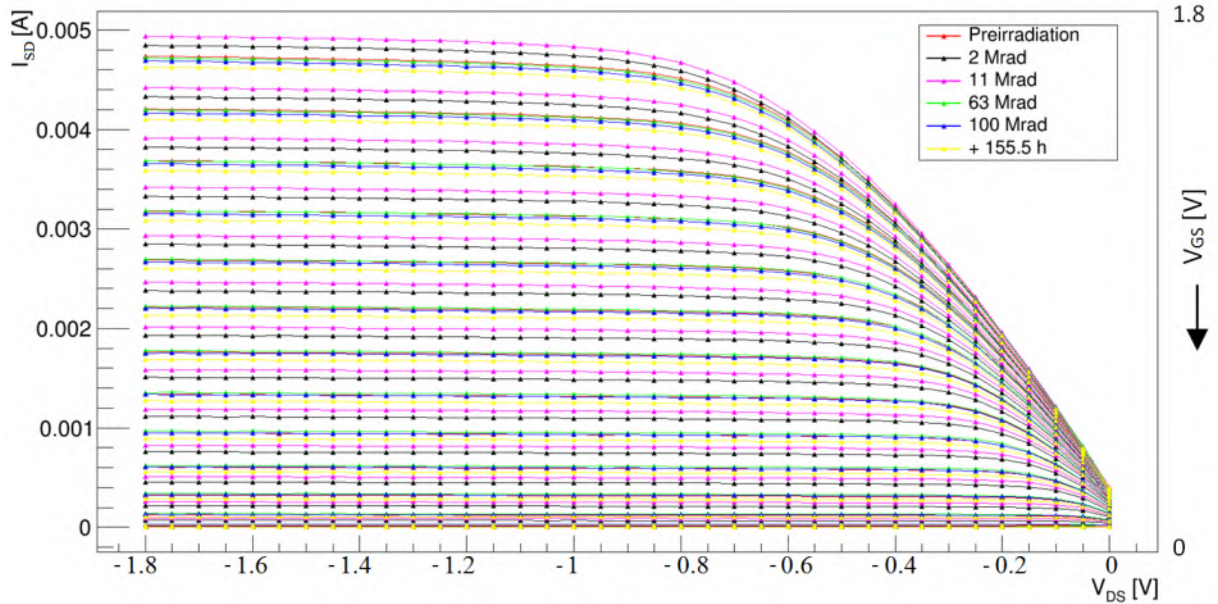



Figure 4.30: IV characteristic of TS2 PMOS with HVP structure in 180 nm CMOS technology for $^{60}$Co radiation dose.

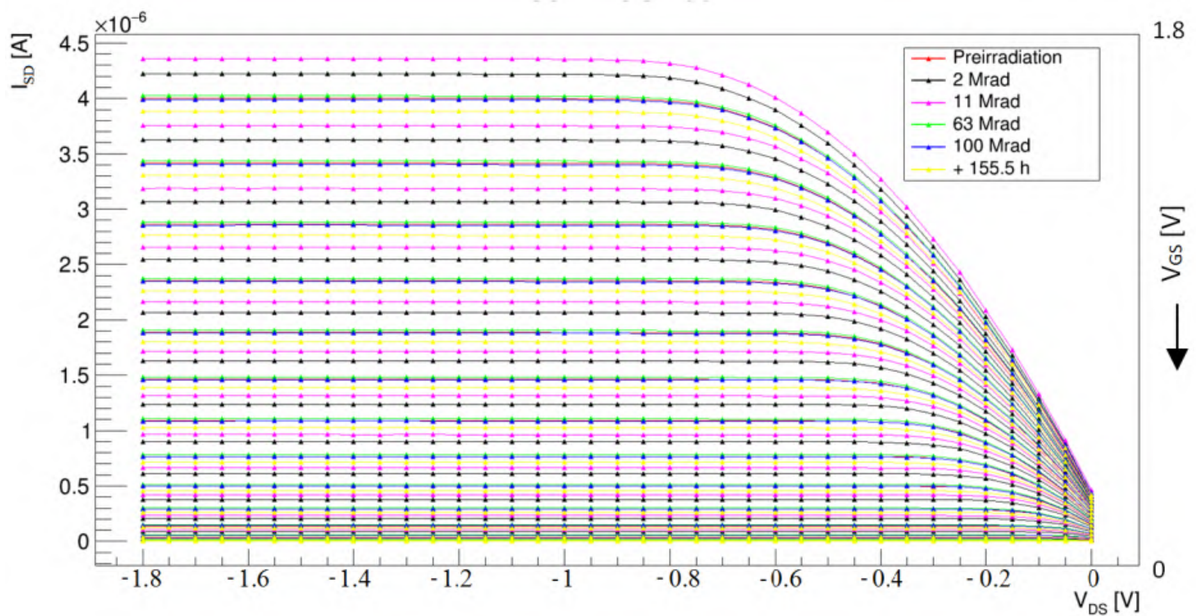



Figure 4.31: IV characteristic of TS3 PMOS with HVP structure in 180 nm CMOS technology for $^{60}$Co radiation dose.

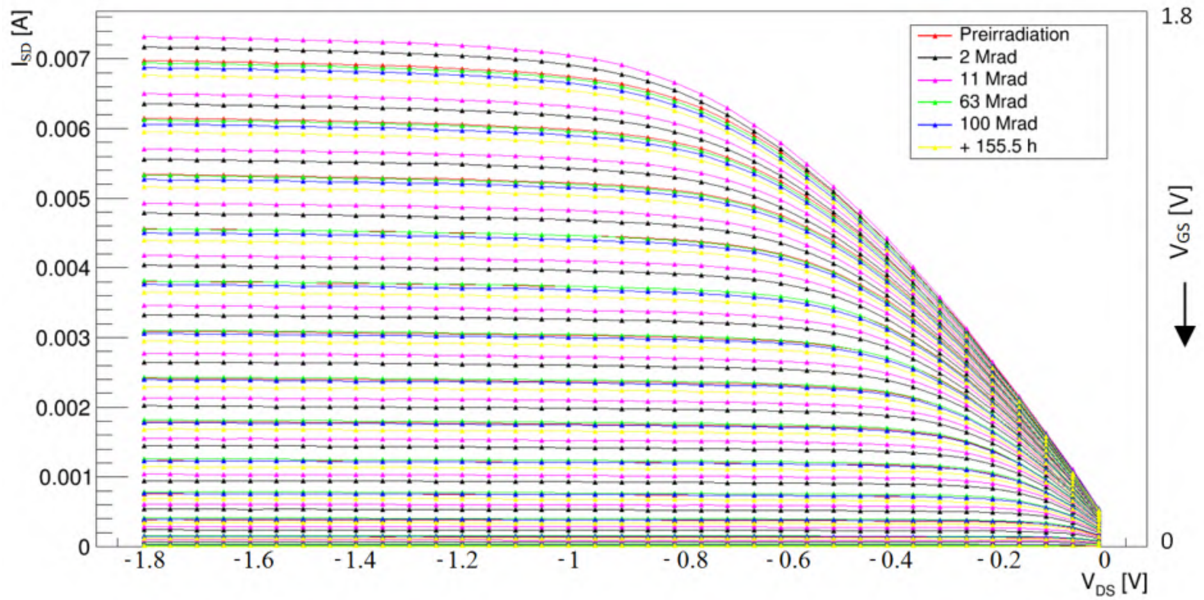



Figure 4.32: IV characteristic of TS4 PMOS without HVP structure in 180 nm CMOS technology for $^{60}$Co radiation dose.

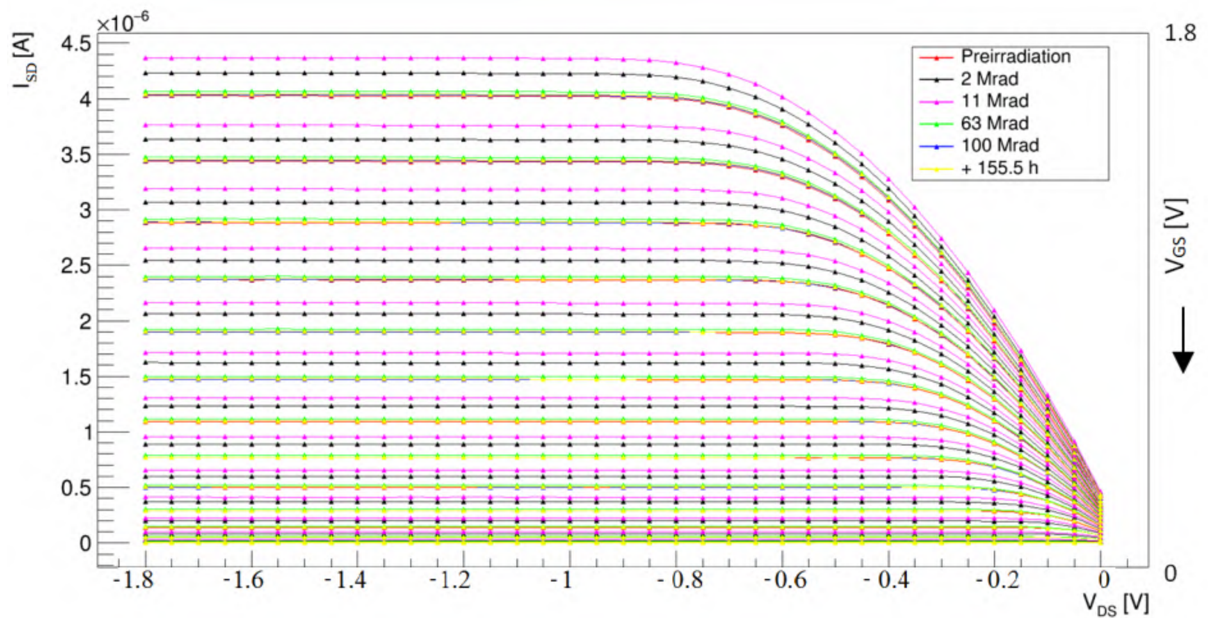



Figure 4.33: IV characteristic of TS5 PMOS without HVP structure in 180 nm CMOS technology for $^{60}$Co radiation dose.

### 4.5.3 IV characterization and capacitance of sensors

One of the key structures in the chip is a circuit for capacitance measurement of the sensor diode. This circuit consists of both pixel types, charge pumps and a 2-bit multiplexer with analogue switches, Figure 4.34. The circuit for precise determination of sensor capacitance layout is shown in Figure 4.35. A pixel with 50 $\mu$m pitch has modified the HV bias ring compared to a pixel in the matrix, where it surrounds all pixels. The IV characterization and capacitance of sensors measurement is described in detail by the author [19].

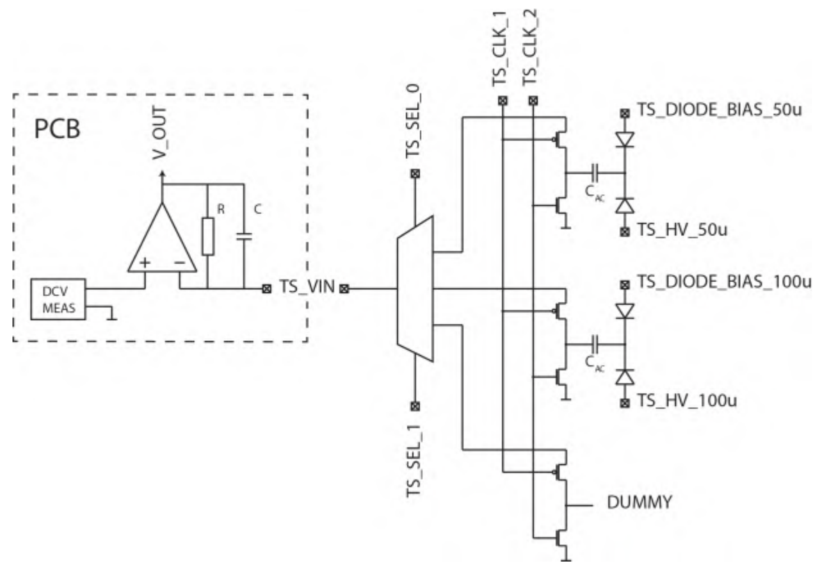



Figure 4.34: Schematic of the circuit for measurement of capacitance of the sensor.

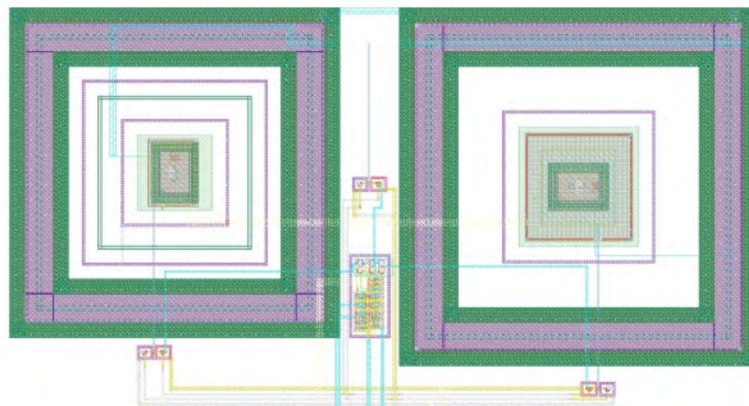


Figure 4.35: The test structure of sensor capacitance. (Middle) DUMMY charge pump.

Figure 4.36 shows the typical IV characteristics of both pixel types with a common connection of sensor diodes (TS_HW_50$\mu$, TS_HW_100$\mu$) and bias diodes (TS_DIODE_BIAS_50$\mu$, TS_DIODE_BIAS_100$\mu$). The measurement of the IV characteristics for each pixel size was proved to be unsuitable, since the IV characteristics are not

comparable to the IV characteristics of the matrices. This is caused by the capacitor of the AC coupling of the pixel electronics architecture. The pixel design requires connection of all bias voltages in the matrices, because a conductive path in the AC coupled capacitor can be created during exposure to ionizing radiation. The X-CHIP-02 with connected bias voltages has 5 to 10 times smaller sensor current than without the connection (depending on the source type and radiation dose). We did not observe hard breakdown during irradiation, but a gradual current increase with sensor bias until a point is reached where the current is no longer constant in time but increases, indicating a thermal runaway phenomenon [87]. This phenomenon is observed for different sensor biases for matrices and diodes, which contains the test structure for sensor capacitance measurement.

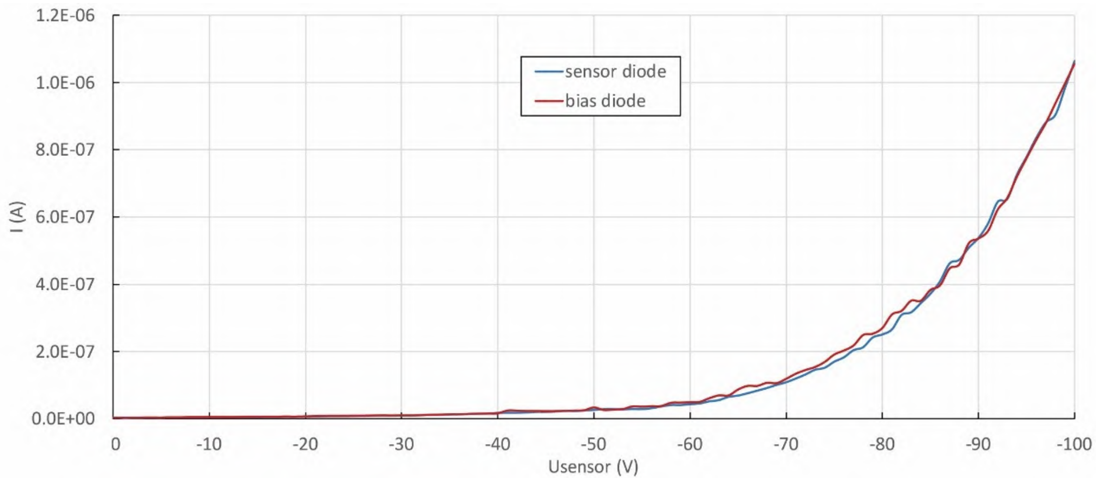



Figure 4.36: The IV characteristic of both pixel types in the test structure [19].

The main purpose of this test structure is to determine the capacitance of a sensitive diode in the MAPS pixel. The resolution of this circuits with $TS_{VIN} = 1.8$ V and switching frequency of 1 MHz is 1.8 nA/fF. An auxiliary circuit, which is on the X-CHIP-02 daughterboard, creates the current to voltage converter with an active RC filter. This converter translates the measurement sensitivity to 1.8 mV/fF. The technique of the capacitance measurement is described by M. Havranek in [29]. The theoretical capacitance of a separate pixel has been with TCAD software simulated. A pixel model has been in TCAD according to the pixel design of the test structure created. For each pixel type, a model of test structure including a single pixel was created. Since there are no adjacent pixels in the model, a 2D simulation is sufficient. The results of the capacitance measurement TCAD simulations are shown in Figure 4.37. The measured capacitance is 2.9 $\pm$ 0.1 fF for 50 $\mu$m pixel pitch and 4.8 $\pm$ 0.1 fF for 100 $\mu$m pixel pitch at negative 100 V. The simulated capacitance of simulation is 3.3 $\pm$ 0.1 fF for 50 $\mu$m pixel pitch and 10.6 $\pm$ 0.1 fF for 100 $\mu$m pixel pitch at negative 100 V. During electrical measurement at negative

90 V, a slight increase of the capacitance due to the connection of the depleted region can be observed, desribed by T. Benka in [19].

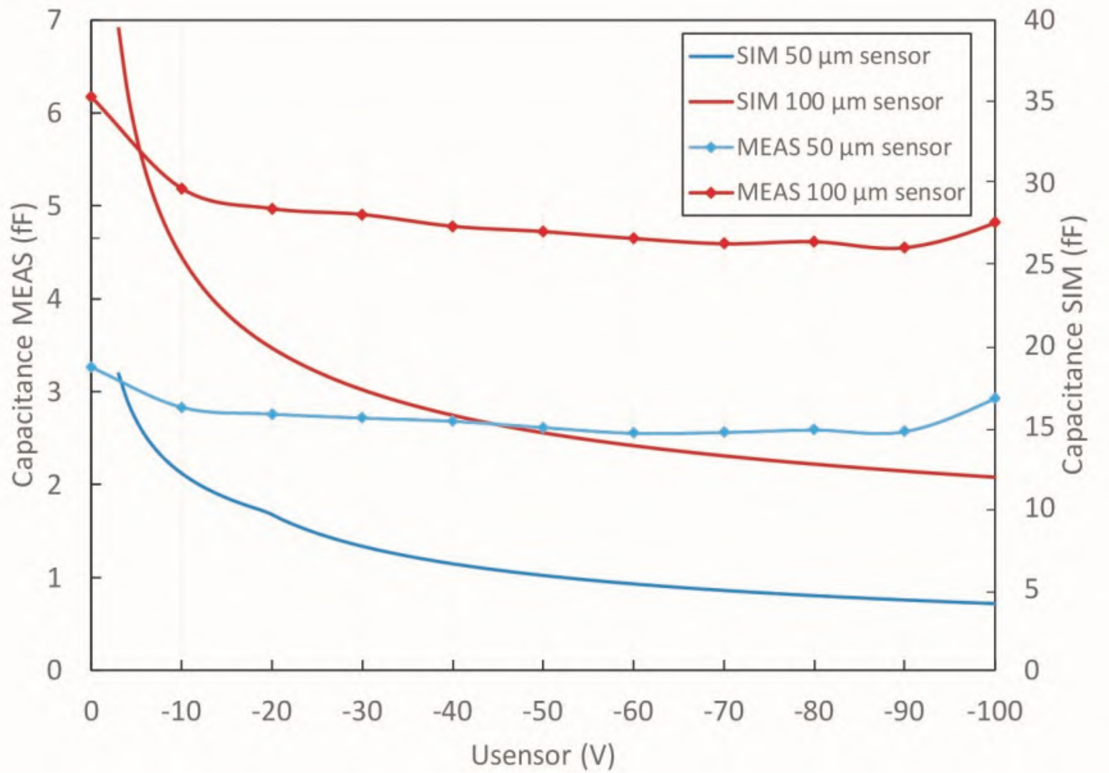



Figure 4.37: Electrical measurement (MEAS) and simulation (SIM) of capacitance of the sensor diodes [19].

The response to an X-ray source is tested and results are shown in this section. The first measurement of the test structures irradiated by X-rays is shown in Figure 4.38 left. There is a marked increase of the sensor current during irradiation and the curves are directly dependent on radiation dose. The sensor current reaches a value of up to 10 $\mu$A with following parameters of the X-ray source: U = 35 kV and I = 100 $\mu$A. In this standard measurement, the detector is irradiated without shielding. Therefore, the positive charge is trapped in the BOX of the whole chip and a conductive channel is formed in the SiO-$SiO_2$ interface. If the detector is covered with a lead shielding with a pinhole, which partially overlaps the HV bias ring area (DTI ring of the matrix with 50 $\mu$m pixel pitch), the sensor current decreases significantly, as shown in Figure 4.38 right. The resulting current value depends on the number of irradiated pixels at the same radiation dose. The pinhole of the lead shielding reduces the number of pixels where the conductive path is created due to irradiation [19].

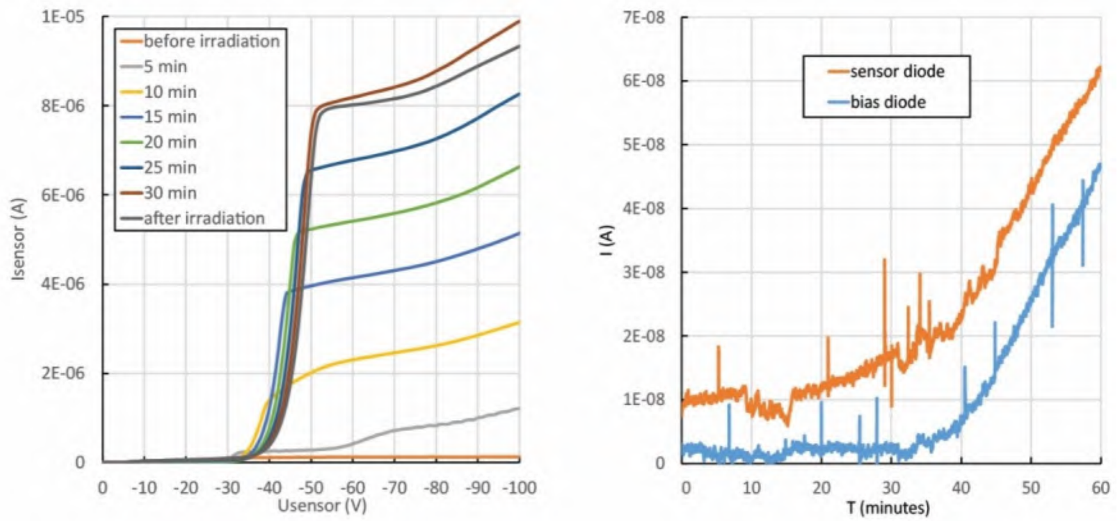



Figure 4.38: (Left) IV characteristic during the X-ray irradiation without shielding. The after irradiation curve represents the measurement made 5 minutes after irradiation. (Right) irradiation with lead shielding and a pinhole in the 50 $\mu$m matrix boundary (HV ring — DTI ring) at negative 50 V [19].

## 4.6 Summary of developed design in 180 nm SOI CMOS technology

The architecture of the proposed design X-CHIP-02 proves to be suitable for increasing the integration density of the pixels electronics and sensor. In the section 4.3 the main advantage of the used architecture and implementation of the topology of the location of the electronics and the sensor on the silicon designed in the 180 nm SOI CMOS has been described. The necessary structure of pixels electronics for the correct function of the detector is shown in section 4.4.

Characterization properties of radiation resistance of test structures is an essential measurement for further research and design of microelectronic structures. An important part of this thesis the radiation damage results of the chip contains transistor structure, subsection 4.5.2, with $^{60}$Co ionization damage and the IV characterization and capacitance of the sensors,subsection 4.5.3, with X-rays has been described.

The ultimate goal of pixel types fo X-CHIP-02 is pixel with 50 $\mu$m pixel pitch, which has a small capacitance (2.9 $\pm$ 0.1 fF by -100 V), relatively little noise, low leakage current (well below 1 $\mu$A at -100 V) and appropriate HV bias ring. The pixel matrix with a 100 $\mu$m pixel pitch was not used for imaging, since many pixels have high noise, described by M. Havranek, T. Benka et al. in [23]. The capacitance of the sensor diodes, simulated in the TCAD, is higher due to ideal parameters of the silicon structure and the parasitic capacitances of the test structure, which have not been included into the simulation model. An important section describing the radiation damage of the chip contains transistor structure with $^{60}$Co ionization damage and results from the X-rays and the TEM.

To achieve acceptable detector sensitivity, a high quality Si-SiO$_2$ interface between the BOX layer and the handle wafer (substrate) must be ensured. An undesirable effect of the trapped positive charge has been observed during irradiation in the Si-SiO$_2$ interface. The IV characteristics during the X-ray irradiation without shielding (Figure 4.38) show the increasing level of the trapped positive charge. If the X-ray source is turned off, the sensor current decreases exponentially by 10 - 15 % in an hour. After 1 hour $\pm$ 10 minutes, the sensor current is stabilized. The stabilization time is affected by the setup settings, technological variations of the chip, X-ray source, etc. The trapped positive charge is proved that the measurement with lead shielding and a pinhole in the HV bias ring area of the detector. The appropriate solution to eliminate this effect is the use of technological process P-STOP and P-SPRAY, as is described in [81].

The transistors test structure consists of eight different transistors which have been integrated in the X-CHIP-02 designed in SOI CMOS. Specific parameters of the transistors

are located in Table 4.1. The main difference is in the modification of the design of test structures with or without HVP. Evaluation of the irradiation test with $^{60}$Co what is crucial for these test structures and for further developments in the technology. Radiation resistance was performed at 100 Mrad with 51 krad/min. About 60 % of the threshold shifts occur during the first 2 Mrad, also a typical phenomenon. Measurements to 100 Mrad on a similar process show a total threshold shift of 25 mV for NMOS with little increase beyond 11 Mrad. Difference between transistors with and without HVP is up to 40 mV. The PMOS structures are a little different then the NMOS structures. Threshold of transistors with HVP is greater by 30 mV than without the HVP. An increase of 100 mV (about 11 Mrad) is resulting from design of PMOS transistor, in detail this issue is solved in [79]. However, slightly less post-radiation degradation has been observed but insignificant. A significant effect of radiation damage is shown in subsection 4.5.2 on Figure 4.26, where is an analog and digital current of the chip. Preirradiation values of the currents have been following: $I_{digital} \approx 400\ \mu A$, $I_{ANALOG} \approx 4$ mA. After 2 Mrad (51 krad/min) the digital current is increased up to 100 mA – 250 times higher.

## 4.7 Measurement with X-CHIP-02

### 4.7.1 Transmission electron microscopy imaging

The next experiment with the chip has dealt with imaging various structures in the X-rays. Only the 50 $\mu$m pixel matrix has been used, because the 100 $\mu$m pixel matrix contains many non-functional pixels. HV bias of the 50 $\mu$m pixels matrix has been – 100 V and their current has been up to 2 $\mu$A. If HV bias is changed to – 20 V, the current is reduced to nA and sensor diode is less sensitive (depleted layer is smaller). The chip was placed in a 15 cm distance from the X-rays source (30 kV, 30 $\mu$A, $e^- \ll 1$ %). Figure 4.39 shows structures of an integrated circuit. These results do not included methods which reduces a pixel noise. The equalization method of pixels represents adjustment of each pixel separately with TDAC.

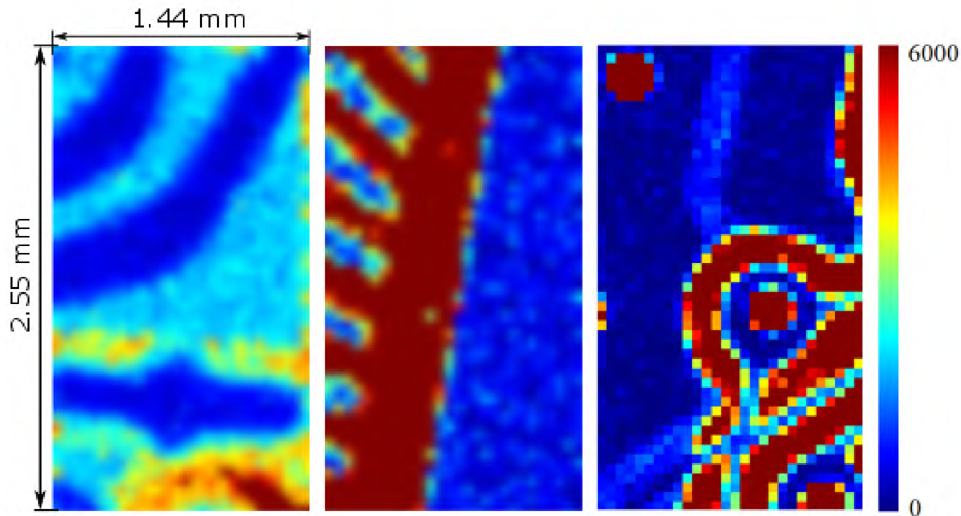



Figure 4.39: Imaging structures with X-CHIP-02 (structure on the right is without interpolation).

Imaging with the X-rays equalization, noise equalization and without equalization have been created by integrating 30 images with the 100 ms exposition, Figure 4.40.

Contrast with and without the equalization using the X-ray source is shown in Figure 4.41, where images are established by integrating 20 images with 100 ms exposition.

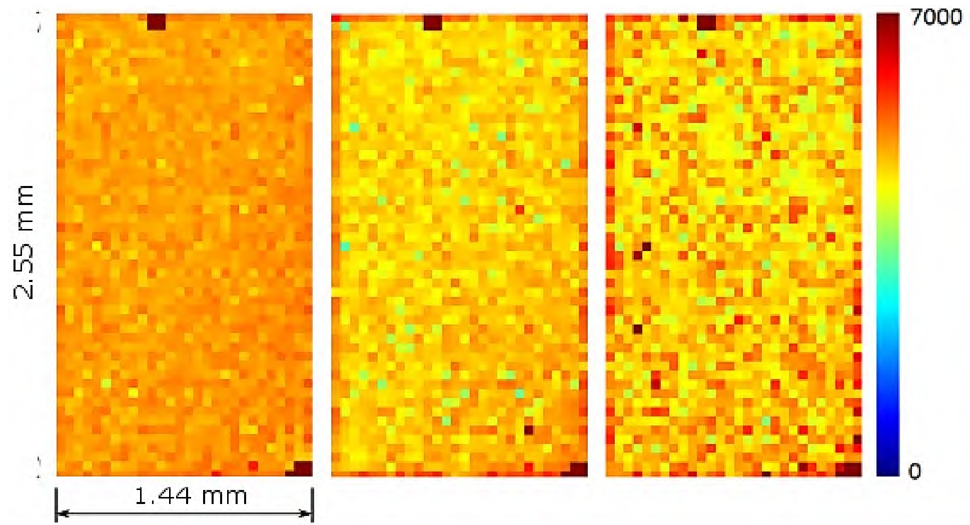



Figure 4.40: (Left) the pixels noise equalization of the X-rays, (middle) the pixels noise equalization, (right) without equalization.

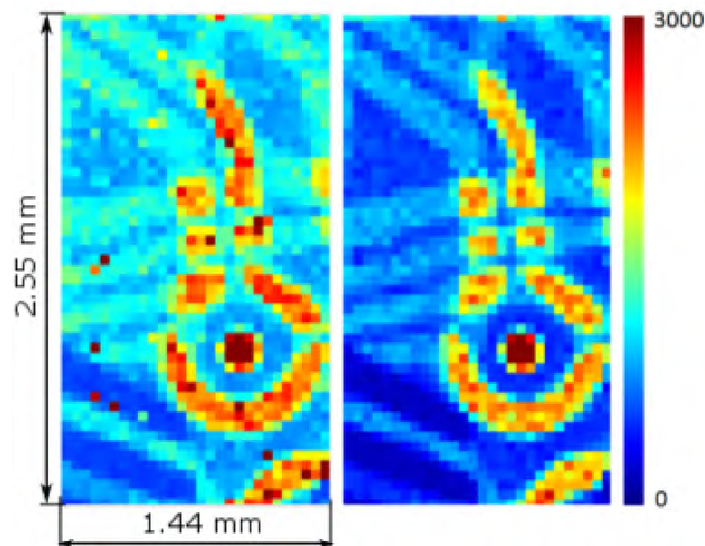



Figure 4.41: Imaging of the X-rays with and without equalization.

The X-rays experiments specified a low dose of electrons ($e^-$). The solution is experiment with the TEM. Figure 4.42 left shows structure in the TEM which is created with the CCD detector of the TEM. Figure 4.42 right is created by integrating 10 images (500 ms – low intensity) with the pixel detector X-CHIP-02 in the TEM. Imaging structure is a carbon foil.

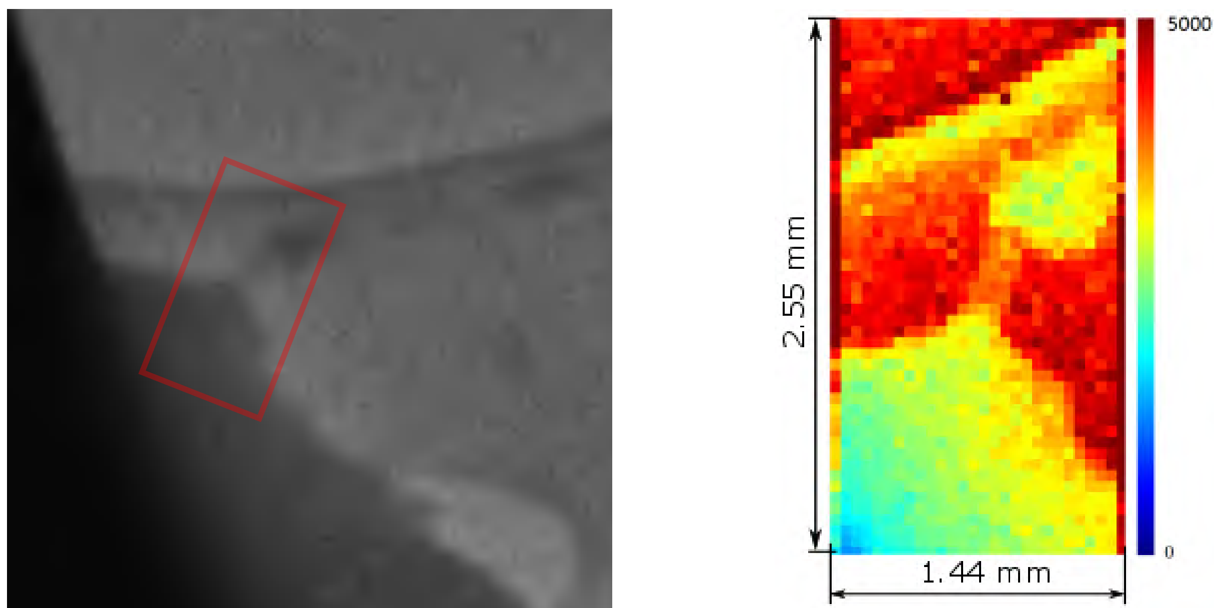



Figure 4.42: (Left) TEM imaging of a carbon foil structures, ($e^-$ imaging). (Right) The X-CHIP-02 imaging in the TEM of a carbon foil structures, ($e^-$ imaging).

Radiation hardness of the X-CHIP-02 was studied by irradiation of the chip with the $^{60}$Co source and consequent measurement of the transistor test structures, subsection 4.5.2.

### 4.7.2 Electron detection measurement

The X-CHIP-02 pixel detector was measured and tested on a Lycan scanning electron microscope [88]. First, the detector was placed on a microscope manipulator and connected by cables to the imported electronics, Figure 4.43.

Figure 4.43: (Left) the cable connector from the detector. The components of the PCB and the solder are suitable for vacuum. (Right) the cable is connected via a wide reducer to the microscope.

Subsequently, the detector was attached and glued to the manipulator using brackets and adhesive tapes to ensure the discharge of the charge. Finally, a foil cover with a hole directly above the chip was placed over the detector so that instead of possible exposure of the PCB board, electrons fell on the foil and grounded as is shown in Figure 4.44.

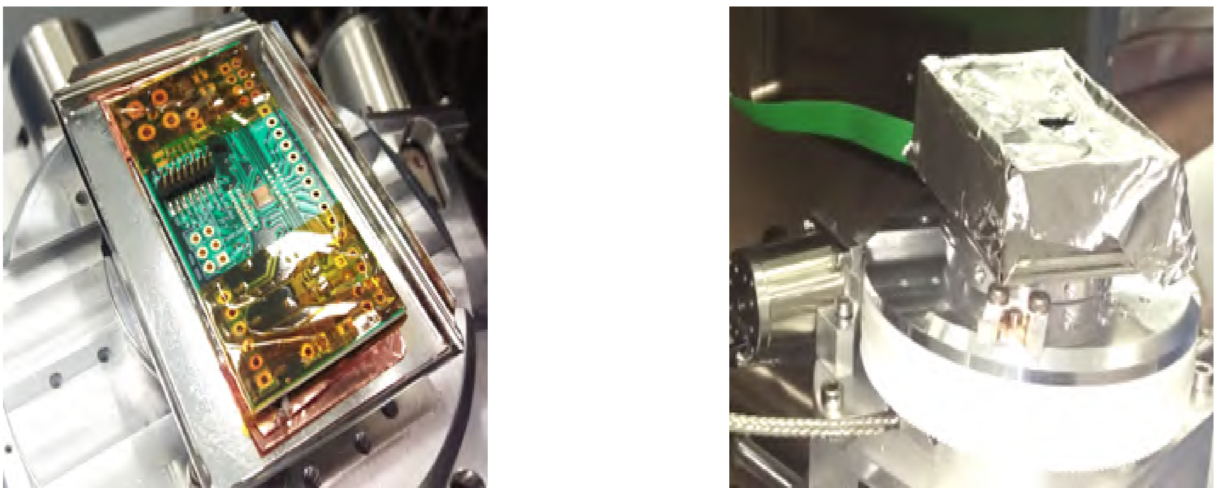


Figure 4.44: (Left) the PCB detector is taped with copper conductive tape and taped with Kapton tape. (Right) A foil cover with a hole above the chip.

As it turned out, aluminum foil was not necessary, but it did not matter either, and even with it, it was possible to observe the image by detecting secondary electrons. There

was only a small local charge with a short illumination of the surrounding PCB board.

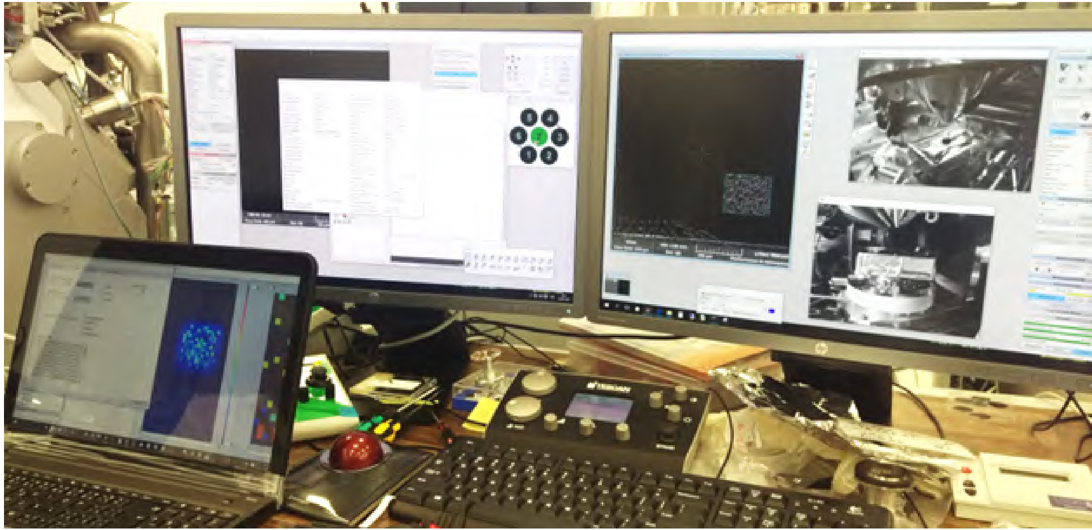


Figure 4.45: Observation of images during measurement. The area where the beam was rasterized at the highest possible speed (10 = 0.1 $\mu$s / pxl) can be seen on the PC monitor. The corresponding rectangular area on the direct detector is visible on the notebook.

The assumption that the detector can withstand exposure to only the lowest sub-picoamp current did not meet, and it was possible to illuminate the chip with a larger current. Most of the following measurements were performed with a current of Beam Intensity (BI) = 5 at an estimate of 45 pA per track. The accelerating voltage was 30kV, Figure 4.46.

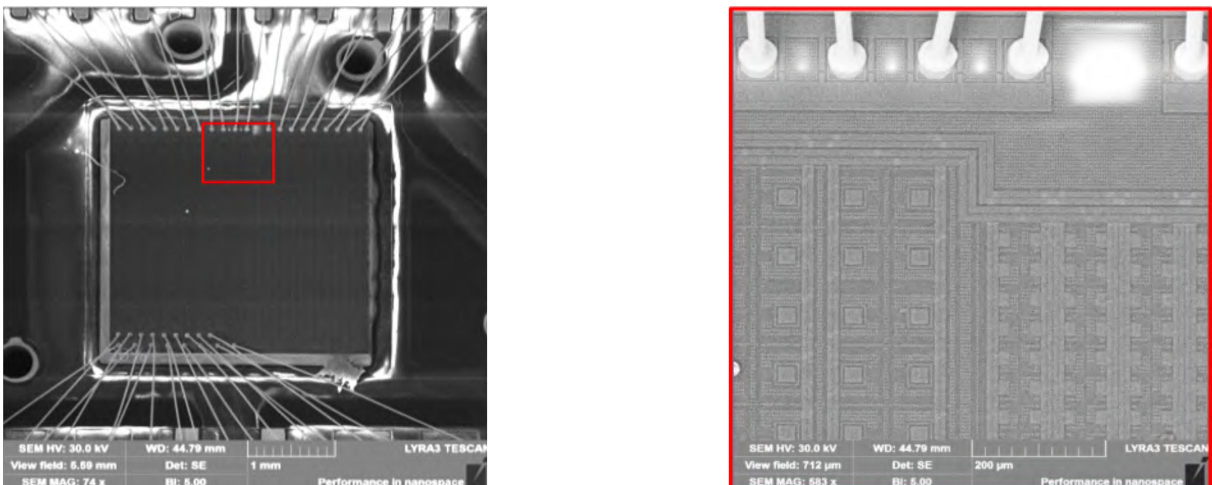



Figure 4.46: (Left) A picture of the whole chip with wirebonds. (Right) a detail of a chip with 100 $\mu$m and 50 $\mu$m pixels.

The Lycan electron microscope allowed the electron beam to expose the required sites on the chip [88]. Measured efficiency of electron detection depending on the beam energy, where at a current corresponding to BI = 5, electrons are detected even at an accelerating

voltage of 10 kV. Furthermore, the efficiency of electron detection was measured depending on the beam's position on the chip. The electron beam was scanned at a very high frequency at the selected location during these tests. When irradiating one site for more than 10 minutes, local radiation damage to the chip occurred when the sensitivity of the given pixels to the electron beam decreased significantly. This place was subsequently visible in the classical microscope observation mode, Figure 4.47. Some oxide layers or other dielectric parts in the chip have been charged. Shortly after the trace appeared, the measurement was postponed to the next day, and the detector was disconnected. The irradiated area was still visible the next day, but a few minutes after connecting the detector, the charge was removed from the charged layer. The sensitivity of the pixels thus marked was still reduced.

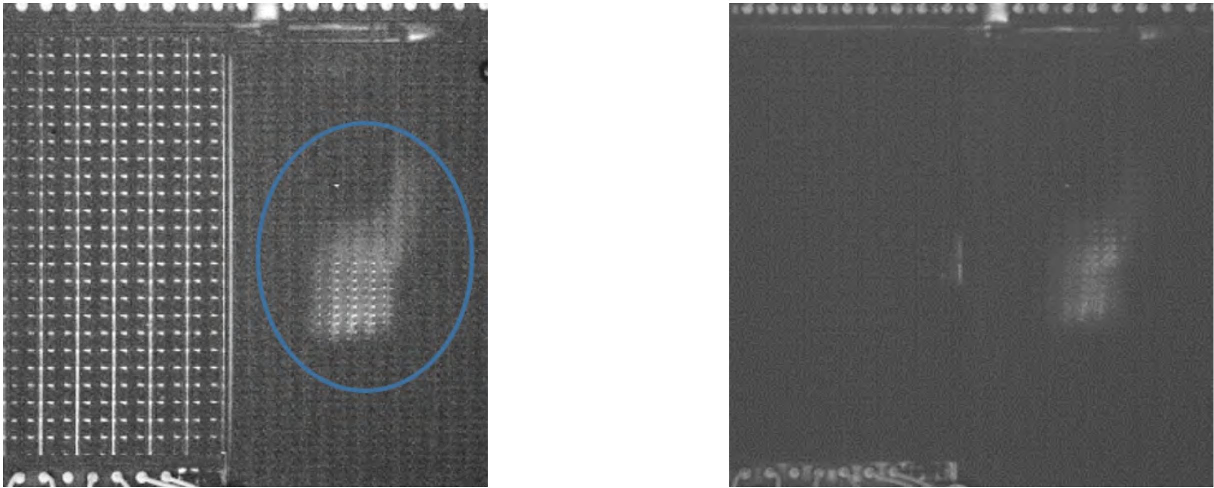


Figure 4.47: (Left) in the ring is the irradiated area after several minutes of irradiation. (Right)The picture of the chip from the second day the chip was disconnected overnight.

Charging of some layers of the chip has been seen in other places. When irradiating larger 100 $\mu$m pixels, certain places near the transistors of all irradiated pixels were periodically charged. The rectangles around the transistors have no particular function, they only serve to planarize the integrated circuit 4.48.

The detector's efficiency is further measured depending on the magnitude of the bias voltage. This voltage changes the size of the discharged area in the silicon and thus affects the spatial resolution of the detector. When testing the detector, the function of the DrawBeam module is used. On the one hand, lines were drawn in different places, next to multiple pixels. Then multiple lines within a row of pixels were drawn 4.7.2.

The main goal was to achieve a prolonged beam movement by pixels. For this purpose, the lowest possible current in the beam has been set. With a further increase in the current in the condenser lens, an even lower total current in the beam was achieved, which corresponded to BI = 0.45 with an estimate of the current in the track at 3.5 pA.

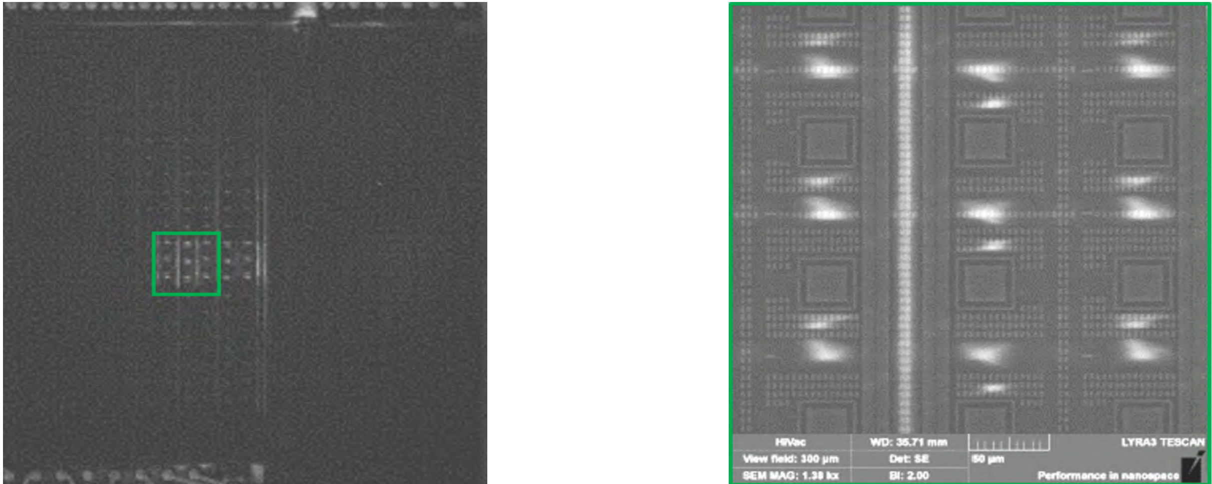



Figure 4.48: (Left) A picture of the chip is taken a few minutes after plugging. (Right) detailed picture of metallization charging.

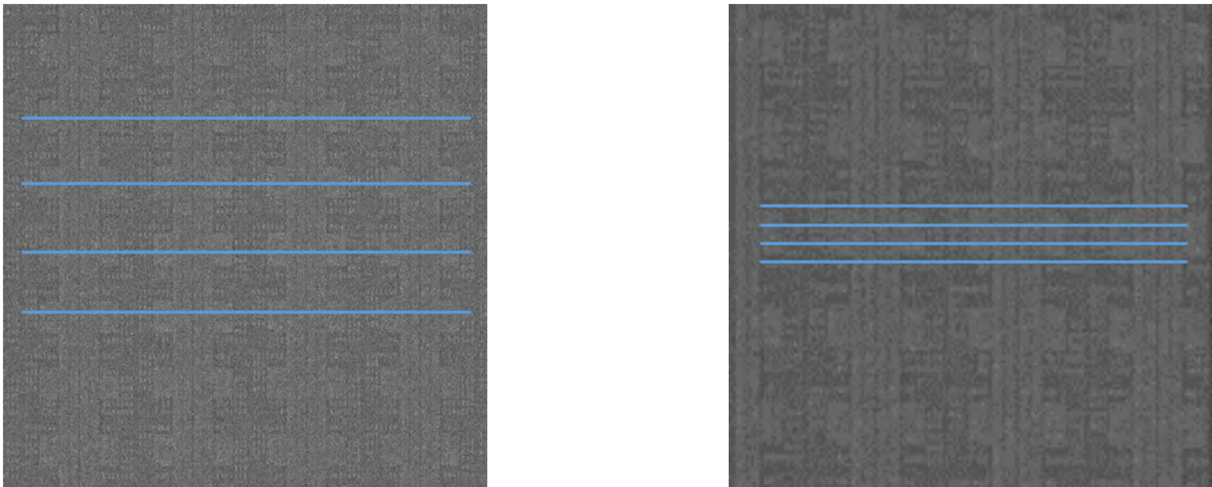


Figure 4.49: On the photos is plotting the beam in lines to measure the detector's efficiency, which is further measured depending on the amount of bias.

Reducing the current alone would not be enough. The beam would still move in a straight line very fast. Thus, a slow shift was achieved in the lithographic mode, when a high total charge dose was set, which is to be deponized per unit area. With the appropriate setting, the track traversed the pixel for more than 5 seconds, the total time of drawing the line was around 3 minutes.

### 4.7.3 Summary of X-CHIP-02 measurements

The prototype of the X-CHIP-02 was successfully tested in industrial facilities, and its parameters are better than just acceptable. An important subsection 4.7.1 describing the radiation damage and imaging with the TEM. The X-rays experiments specified a low dose of electrons ($e^-$). Figure 4.42 left shows structure in the TEM which is created with the CCD detector of the TEM. Figure 4.42 right is created by integrating 10 images (500 ms – low intensity) with the pixel detector X-CHIP-02 in the TEM. Imaging structure is a carbon foil. The imaging pixel detector to be a suitable candidate for another application has proven, as focal imaging to determine the lifetime of an X-ray device.

The electron detection measurement in the characterized the radiation tolerance of the subsection 4.7.2 X-ray source, $e^-$. The main goal was to achieve a prolonged beam movement by pixels. The main goal was to achieve a prolonged beam movement in pixels to determine the area where the non-resilient charge is maintained. The duration and behavior of the irradiated region after re-switching on the detector were further described. This measurement develops as the TEM the usability of the detector in X-ray imaging applications.

# Chapter 5

# Blocks designed in various technologies

This section represents the blocks which have been designed in other technologies and are suitable for a future prototype of the X-CHIP. The individual blocks and technologies are described in following section. The test structure LVDS designed in 150 nm CMOS technology is described in section 5.1. The introduction of the X-CHIP-03 prototype and elecrical measurement of the LVDS is described in section 5.3. The third prototype of the LVDS drivers is in section 5.4. Funktionality and desing of the X-XHIP-03, section 5.3, have been published by the author with a percentage uniform distribution for all the authors mentioned

- M. Havranek, T. Benka, M. Hejtmanek, *et al.*, "X-CHIP-03: SOI MAPS radiation sensor with hit-counting and ADC mode", in *2018 IEEE NUCLEAR SCIENCE SYMPOSIUM AND MEDICAL IMAGING CONFERENCE PROCEEDINGS (NSS/MIC)*, IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Sydney, AUSTRALIA, NOV 10-17, 2018, IEEE Nucl & Plasma Sci Soc; IEEE, 2018, ISBN: 978-1-5386-8494-8

and the LORDS design, section 5.4, of a capacitor DAC for charge redistribution analog to digital converter with successive approximation have been published by the author with a percentage uniform distribution for all the authors mentioned:

- P. Vancura, M. Havranek, T. Benka, *et al.*, "A capacitor dac for charge redistribution analog to digital converter with successive approximation", cited By 1, vol. 343, 2018

The first prototype designed in 65 nm CMOS technology is described in subsection 5.5.1 and the second modified prototype in subsection 5.5.2. Funktionality and desing of the subsection 5.5.1 and subsection 5.5.2 have been published by the author with a percentage uniform distribution for all the authors mentioned:

- F ARTECHE GONZALEZ, N BACCHETTA, T BENKA, *et al.*, "Extension of RD53", CERN, Geneva, Tech. Rep., 2018, Don't have official titles of Project manager and Technical Coordinator. Entered CERN co-spokesperson as project manager (responsible for team account) and Project Engineer as Technical Coordinator. [Online]. Available: `http://cds.cern.ch/record/2637453`

## 5.1 Low-Voltage Differential Signaling transmitter / receiver designed in 150 nm CMOS technology

The X-CHIP-02 has one important constraint in the communication. The chip generates too much data and its data transfer from / to the chip is unsatisfactory. Only the Single-ended transmission has been used in the chip design, a detailed decription of the Single-ended transmission is in the LVDS Application and Data Handbook [91]. The solution of low data througput is the LVDS which is well described in [91], [92]. The LVDS is designed and manufactured in 150 nm technology. These blocks are standardized under ANSI/TIA/EIA-644, from [93], [94], and consist only of 3.3 V transistors. The transmitter comprises of a current-mode driver which has variable strength, as shown in the Figure 5.1 [95].

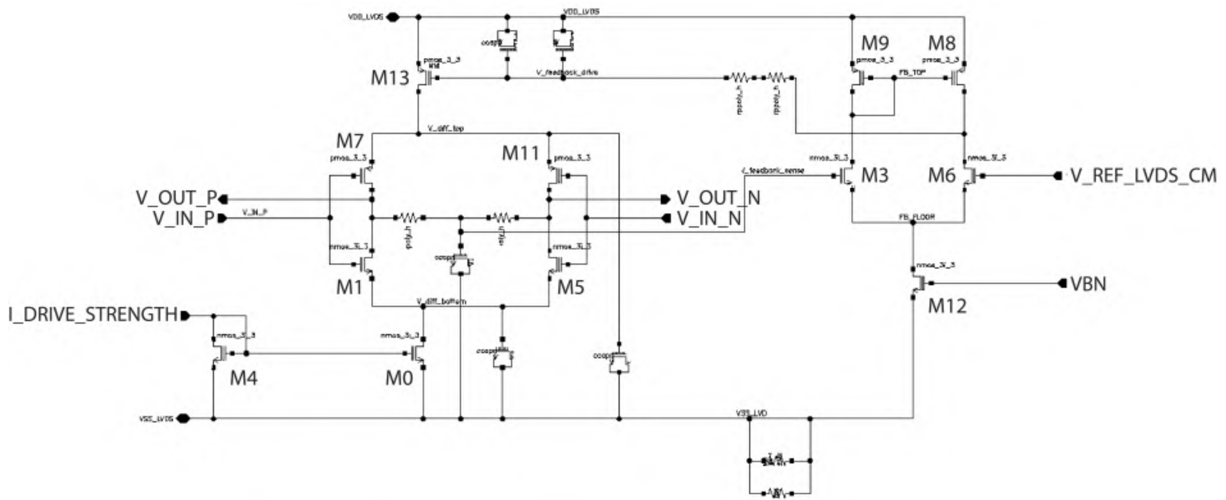



Figure 5.1: The LVDS transmitter in 150 nm CMOS technology.

A basic element of the receiver is differential amplifier. The differential inputs are divided into two diff-pairs of the diff-amps (M10, M24 and M12, M25, as shown in Figure 5.2) and their output constitutes the output diff-pair of the output diff-amp (M14 and M26). Current sources gates (M11, M13 and M15) are linked with NMOS current, electrons in NMOS transistors are faster as PMOS transistors. An accurate resistor with

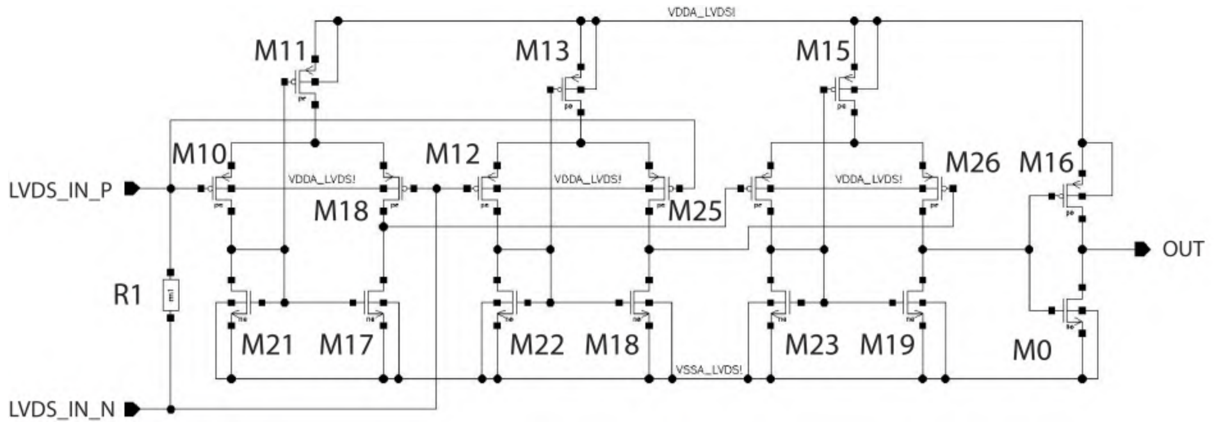



Figure 5.2: The LVDS receiver with output invertor in 150 nm CMOS technology, R1 = 100 Ω.

a value of 100 Ω is connected in parallel to the input, which is terminates the line and converts current to voltage.

Specification of the LVDS block has been measured at the different frequencies with specific capacitance 0.1 pF, as shown in Figure 5.3. At different frequencies has been sent over the transmitter Field Programmable Gate Array (FPGA) 1024 bits long chain to the receiver (LVDS integrated circuit). The transmitter of the chip sends back the string into the FPGA, where the chains are compared.

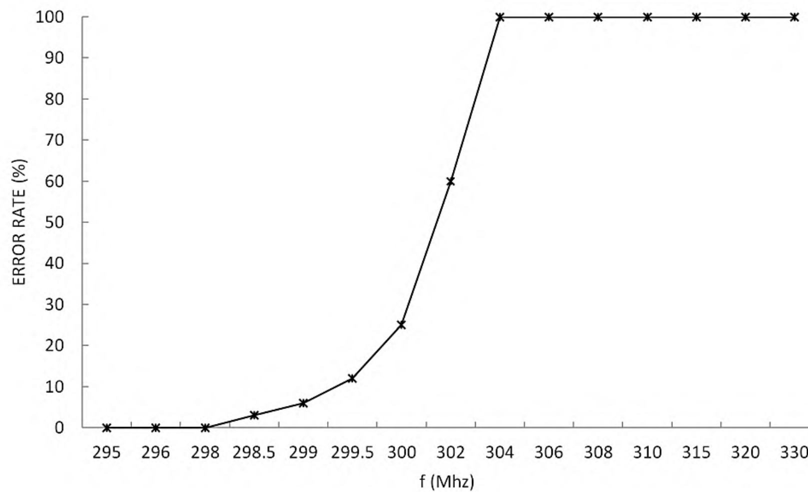



Figure 5.3: The LVDS receiver with output invertor in 150 nm CMOS technology, R1 = 100 Ω.

## 5.2 Summary of LVDS designed in the 150 nm CMOS technology

The first prototype ofthe LVDS drivers designed in 150 nm CMOS technology has been described which the layout has been designed in collaboration with colleague Ing. Gordon Neue. The detailed functionality of the schematic architecture of the receiver and transmitter is described in section 5.1 and measured by the author. The maximum stable frequency without errors of the communication measurement with the FPGA forms 298 MHz. The main disadvantage of this technology was the vehement closure of the manufacturer due to financial reasons, so it was no longer possible to continue with this technology. The electrical measurement of the microelectronic structure of LVDS has not been performed due to damage and lack of the sample prototype.

## 5.3 X-CHIP-03

The LVDS drivers for the X-ray imaging pixel detector X-CHIP-03, described by M. Havranek and T. Benka et al. in [25], have been developed using a 180 nm deep submicron Silicon On Insulator (SOI) CMOS commercial technology. The X-CHIP-03 is a Monolithic Active Pixel Sensor (MAPS) and its architecture is based on the first prototype X-CHIP-02 with hit counting. The advantages, design, features, test structures and measurements of the first prototype X-CHIP-02 fabricated in SOI CMOS technology have already been described in previous chapters and published by T. Benka [19]; M. Havranek, T. Benka et al. in [23] and M. Marcisovska, T. Benka et al. in [24].

The applicability of the X-CHIP-02, section 4.2, has been found for many commercial applications, for example the imaging detectors in medicine industry, detectors for dosimetry and spectroscopy, tracking detectors, etc. However, all of them require to improve the speed of data acquisition from the detector. The communication speed and its radiation resistance is the one of the most important parameters of the detector. The X-CHIP-02 communication consists of long shift register daisy chaining all pixels, subsection 4.4.3. This architecture limits the maximum data rate below 50 kbps. The LVDS transceiver and receiver allow to increase the speed of communication to 500 Mbps with respect to low power consumption (6 mW) and radiation resistance. The motivation for development the LVDS IP block is the utilization of the detector in the commercial application. The LVDS receiver and transmitter are included in the X-CHIP-03 detector. The design of the LVDS IP blocks, as well as circuit simulation, laboratory measurement technology are described in the following chapter. The experimental results are of great importance for further development of the LVDS communication with radiation tolerance design which is intended for MAPS sensors in SOI technology. The X-CHIP-03 PCB daugther boar with respect to the required line impedance 5.4.

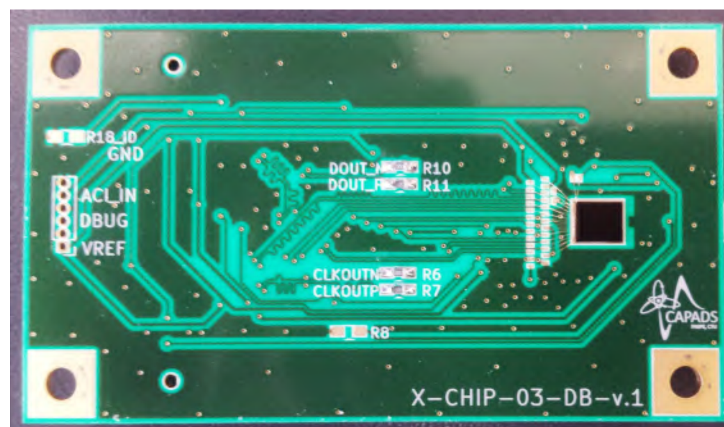



Figure 5.4: The CHIP-03 PCB dagther board with respect to lines impedance.

### 5.3.1 Low-Voltage Differential Signaling transmitter / receiver designed in 180 nm SOI technology

In the X-CHIP-03 are included following LVDS IP blocks: transmitter and receiver. These blocks are standardized under ANSI/TIA/EIA-644 and complited only of 1.8 V - transistors [93], [94]. The first prototype of the IP block prototype has been fabricated in 150 nm, section 5.1, technology which forms the test structure in integrated circuit PHPix [28].

The transmitter comprises of a current-mode driver which is variable, Figure 5.6 and its architecture is based on the LVDS driver designed in 150 nm technology, section 5.1, Figure 5.1 and as is described in [96]. Linear current regulator (the transconductor circuit) represents the IP block, which allows to adjust the current-mode from 3.5 mA to 9 mA (LVDS_STRENGTH) and its connected to the gate of M2 transistor (VBN_LVDS). In this scheme is a significant addition of the feedback [96]. The LVDS driver in the X-CHIP-03 was successfully simulated up to a frequency of 285 Mhz during the simulation in the corners that define the various conditions of the circuit as changes in voltage or temperature.

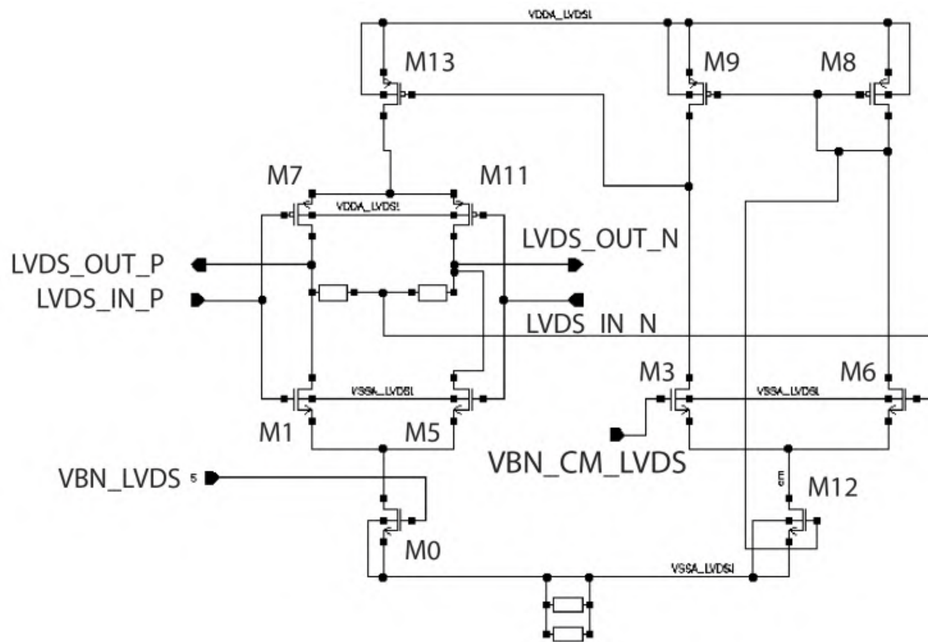



Figure 5.5: The CHIP-03 LVDS transmitter schema with adjustable current strenght designed in 180 nm SOI technology.

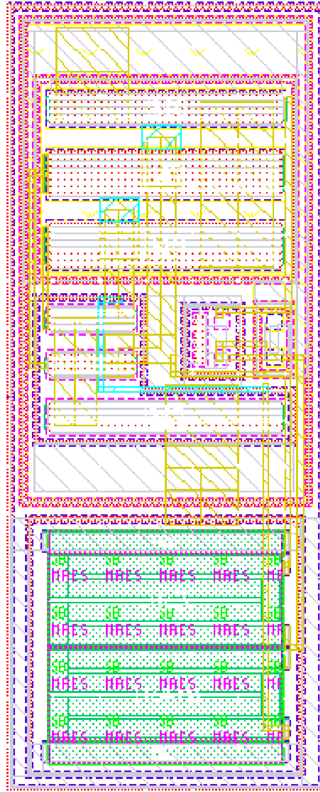


Figure 5.6: The CHIP-03 LVDS transmitter layout in 180 nm SOI technology.

Specifications of the LVDS blocks in the X-CHIP-03 is measured at the different frequencies and LVDS_STRENGTH (LS). The measurement is performed by a high frequency differential probe uitable for this measurement. Figure 5.7 shows the eye diagram of the LVDS at frequency 50 MHz and LS = 110 and Figure 5.8 at f = 50 Mhz and LS = 170. LS adjustment for 3.5 mA is not acceptable because the common mode voltage does not meet the LVDS standard. The LS is convert to digital value in the shift register where the 3.5 mA in the transconductor represets the value of 173 and 9 mA the 112.

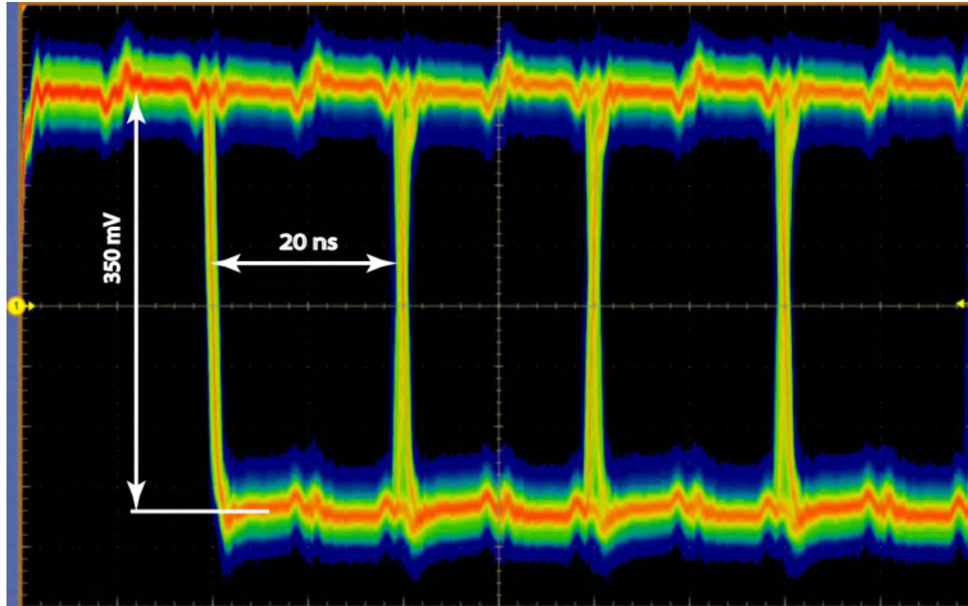



Figure 5.7: The electrical measurement of the CHIP-03 LVDS driver at 50 MHz and LVDS_STRENGTH 110. The common mode voltage is 350 mV at 50 mV/div.

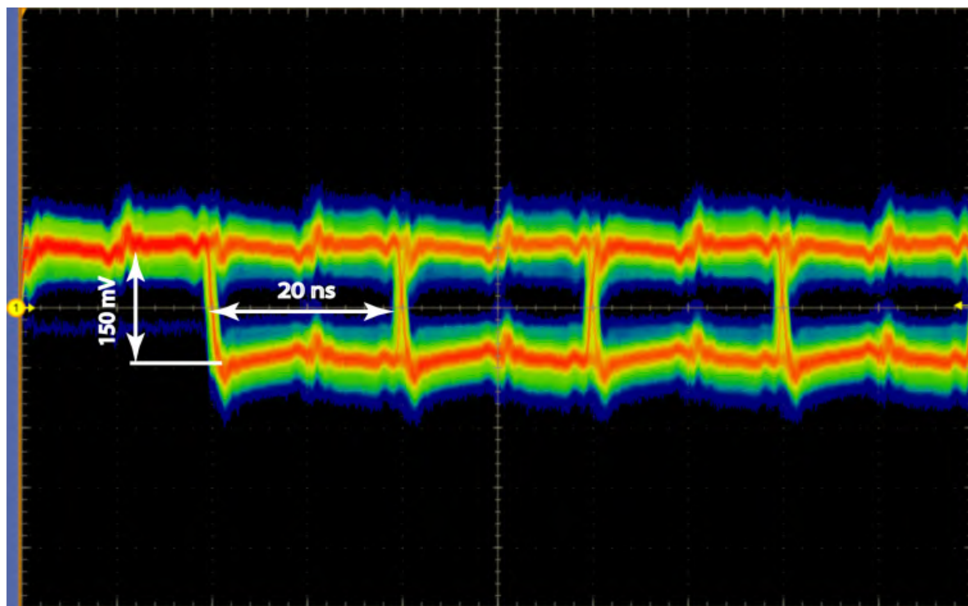



Figure 5.8: The electrical measurement of the CHIP-03 LVDS driver at 50 MHz and LVDS_STRENGTH 170. The common mode voltage is 150 mV at 50 mV/div.

On the Figures 5.9 and 5.10 are shown the eye diagram at frequency 100 MHz and LS = 100 and 170. The common mode voltage decreases with increasing frequency due to incorrect layout design. After an additional detailed simulation of the extracted layout with parasitic capacitances and resistances, it turned out that the power supply of the LVDS driver does not have sufficient dimensions, so at higher frequencies when the LVDS driver is loaded, the resistivity of the supply metallization increases. The mea-

surement of the LVDS communication is shown in the Figure 5.11. The yellow signal presents the LVDS output fo the chip. In the beginning, the frequency is 200 MHz and gradually decreases with stepf of 2 MHz. The increase of the common mode voltage is due to a transient phenomenon caused by the capacity of the transmitter input transistors. Hovewer, the communation by frequency from 100 MHz to 200 MHz (maximum measurable frequency) is not stable, the configuration has errors and is unusable.

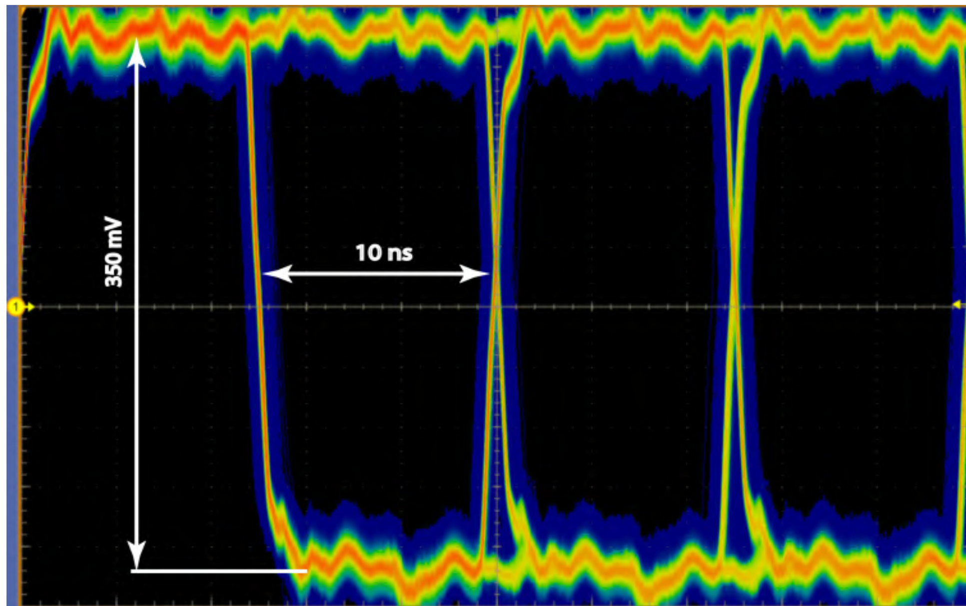



Figure 5.9: The electrical measurement of the CHIP-03 LVDS driver at 100 MHz and LVDS_STRENGTH 110. The common mode voltage is 350 mV at 50 mV/div.

The Row Shift Register shifts the correct data. However, communication is possible at the critical speed of 100 MHz. The frequency limit is caused by the design of the LVDS receiver, in a new version of the ASIC the LVDS transceiver is redesigned, the LORDS pixel detector. The input levels of the LVDS receiver are in saturation and the current source for these stages is not sufficient, Figure 5.12. The second problem with communication is the impedance adaptation of the daughter PCB, where the chip is wire-bonded. The daughter PCB consists of decoupling capacitors for power supplies and connectors for connecting the motherboard (FPGA board). The circuit parts validated in the X-CHIP-03 testing ASIC design are working according to the requirements except the LVDS transceiver, which was redesigned for the new version of the ASIC.

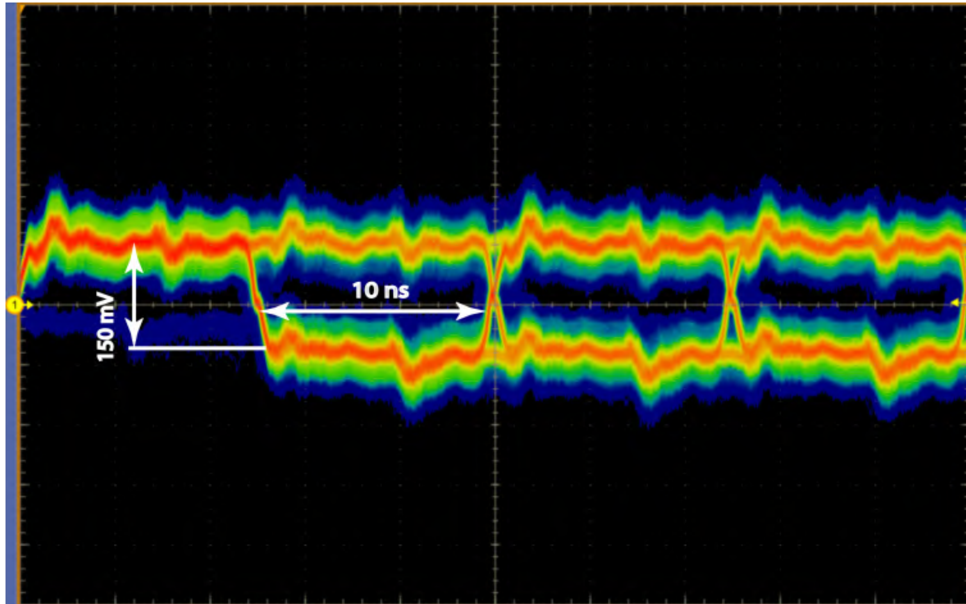



Figure 5.10: The electrical measurement of the CHIP-03 LVDS driver at 100 MHz and LVDS_STRENGTH 170. The common mode voltage is 150 mV at 50 mV/div.

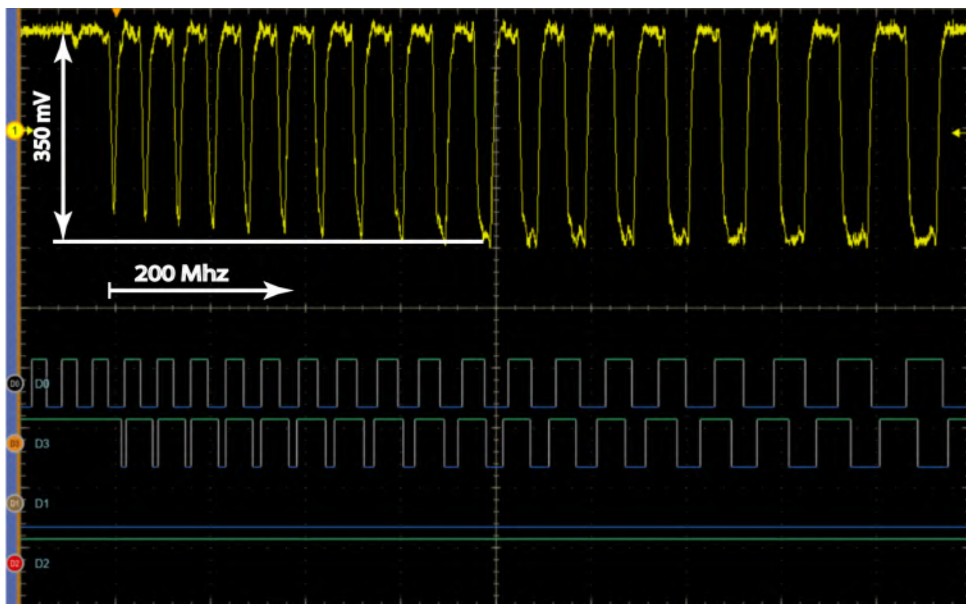



Figure 5.11: The electrical measurement of the CHIP-03 LVDS driver at frequency drop from 200 MHz and LVDS_STRENGTH 110, 200 mV/div. The yellow and third curve (D3) is the output of the LVDS transmitter, second curve (D0) is the clock output from the FPGA and the input for the LVDS receiver.

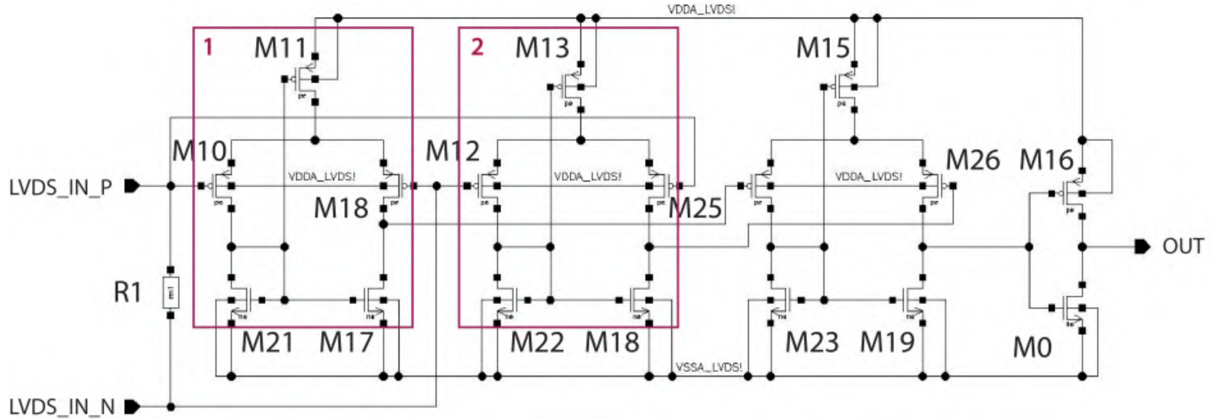



Figure 5.12: The LVDS receiver design of the X-CHIP-03, the red boxes are the input stages of the receiver.

### 5.3.2 Summary of X-CHIP-03 LVDS designed in the 180 nm SOI CMOS technology

The second the X-CHIP-03 prototype of pixels detector contains a single pixel matrix with 50 $\mu$m pixel pitch which in X-chip-02 has been verified, section 4.7. The first microelectronics cirtuis of the LVDS was designed in 150 nm CMOS technology and the architecture with fundamental transformation into another technology for the X-CHIP-03 has been used and developed by the author, described in section 5.1. The necessary simulation and electrical measurements are contained in subsection 5.3.1. The maximum frequency 200 MHz for successful differential communication due to narrow metalizations paths of the supply power in the layout and impedance mismatch has been verified. The LORDS prototype verified the electrical measurement of the LVDS drivers in the X-CHIP-03 in the simulations of the LVDS. The frequency of 200 MHz to 500 MHz in the simulation of complete communication with shift registers, with extracted parasitic capacitances and resistivities, has been increased by design modification in the layout.

## 5.4 LORDS

The radiation tolerance is considered the main obstacle for space research with cosmonauts and in the colonization of the Solar system. The orbit radiation has a destructive effect for the electronic systems (unreliability, Single Event Upset (SEU), degradation of component properties), device mechanics (natural damage) and naturally to the living organism, including humans. The ionizing radiation properties in the universe are qualitatively different from the terrestrial radiation sources. Therefore, the cosmic dosimetry concerning the instrumentations and effects is very different from the terrestrial dosimetry.

Since the end of the Apollo mission, human-flight is conducted in the LEO, where Earth's magnetosphere considerably protects astronauts. Flights beyond the LEO boundary, which are planned for the next decade by space agencies and private companies, are complicated due to radiation damage. A compact device that allows for the measurement of not only regular dosimetric quantities, but also the determination of the type of ionizing radiation and the biologic effect of radiation, is highly demanded by space agencies. The other required property of the device is the detection of the fast neutrons from energy events of the Sun magnetosphere, which can be a precursor to the arrival of a cloud of charged particles from the solar eruption and provides early warnings to the cosmonauts.

The MAPS, which is a revolutionary monolithic ionizing radiation detector, significantly improves the detection of physical parameters and enables new types of measurement of physical quantities. A unique type of the dosimetric MAPS sensor, Lightweight Orbital Radiation Detection System (LORDS), was developed using a 180 nm deep submicron CMOS commercial technology, chapter 4. The design of LORDS, as shown in Figure 5.13, as well as overall layout design and circuit simulation of whole detector and the LVDS driver and pixel sensor architecture, has been developed by the author and is presented in subsection 5.4.1. The experimental and simulation results are of great importance for the further development of the dosimetric MAPS detector, designed in SOI technologies, for space applications. However, no experimental measurements were performed of the LORDS.

The technological architecture sensor elements of the LORDS is in section 4.3 and 4.6. The largest part of the sensor area is occupied by the pixel matrix which is sensitive to radiation and holds the analog information about the signal amplitude. The pixel matrix is read out row by row. In ADC mode, the memorized pixel peak voltages by Peak Detector Hold (PDH) are transferred to the 64 Analog to Digital Converters (ADC) and digitized, Figure 5.14. The ADC parameters are following: 10 bit resolution, 250 kS/s speed, P = 150 $\mu$W, area: 57.5×482 $\mu m^2$ and $V_{ref}$ is 1024 mV, described by P. Vancura, T. Benka et al. in [89]. The digitized data are then transferred to the shift register and transmitted outside the chip by communication LVDS or CMOS. The architecture of

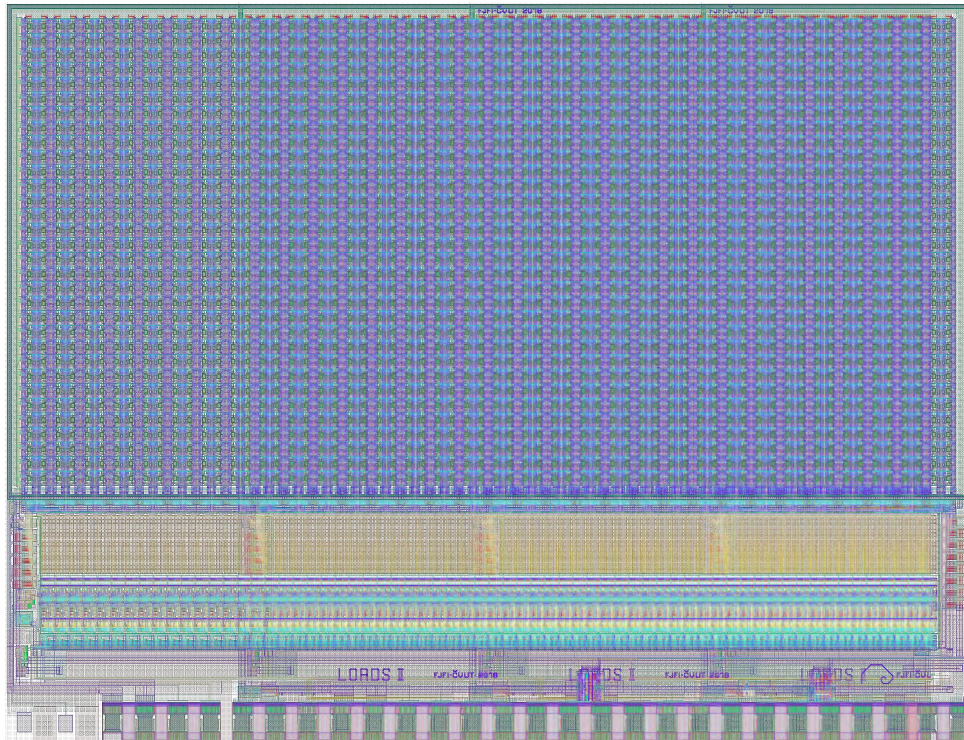



Figure 5.13: The layout of the LORDS.

the LORDS is designed from the previous prototype the X-CHIP-03 which is described by M. Havranek and T. Benka at al. in [25].

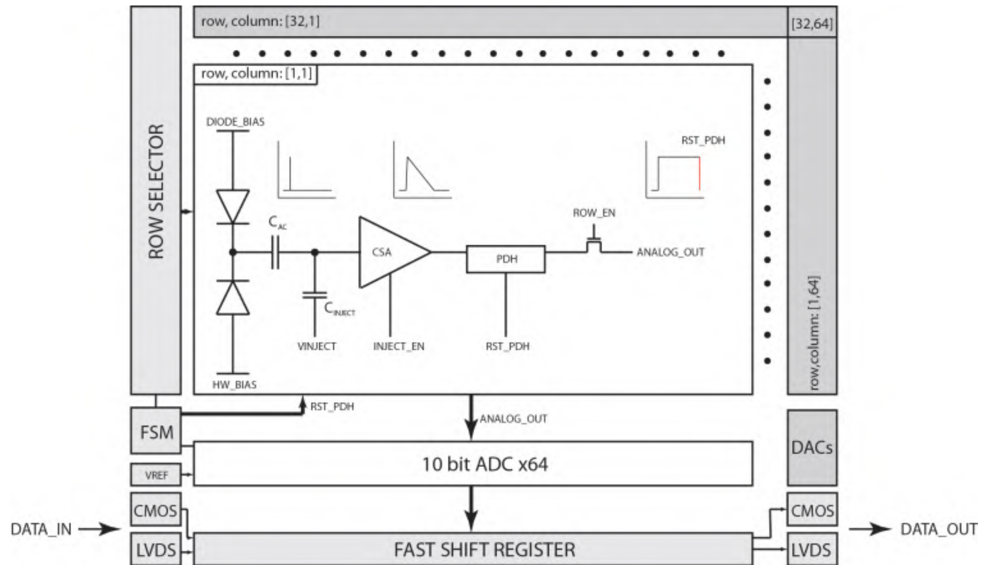



Figure 5.14: The LORDS communication architecture.

The blok diagram of the pixel design is shown in Figure 5.15. The main modification of the LORDS detector is a novel concept of the sensor element. The pixels consist of the octogonal sensor implant into handle wafer, injection, CSA, PDH and output enable. The octonogal sensor has the main advantage in the density of the electric charge in the hanle-wafer. With the standard sensor design, the edges of the electric charge density are sharp during the simulation. One of the requirements of the sensor is the homogeneity of the magnetic field of adjacent sensors in the handle wafer, which the octagonal sensor can largely eliminate 5.16.

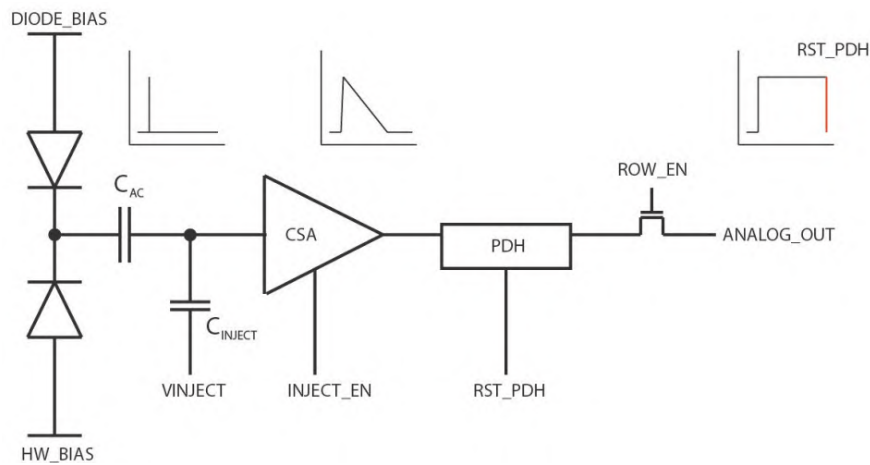



Figure 5.15: The pixel block diagram of the LORDS.

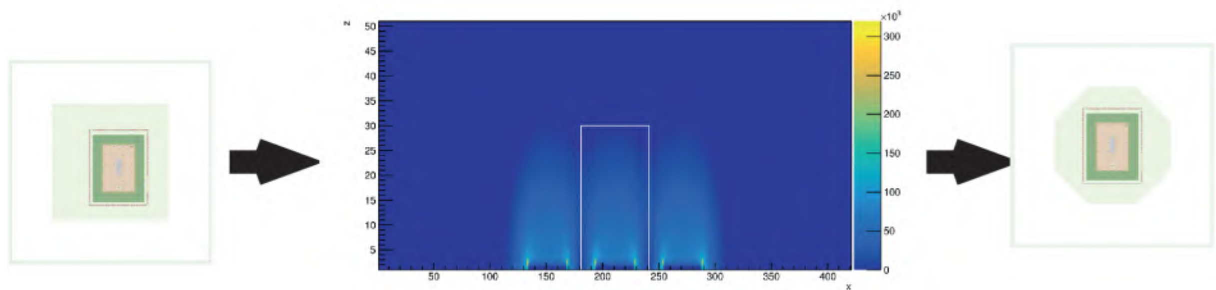


Figure 5.16: (Left) the standart sensor design in the X-CHIP-02 and X-CHIP-03. (Middle) the density of the electric field with the standard sensor design, three pixels with 50 $\mu$m pixel size. (Right) the octogonal sensor design in the LORDS.

The CSA has range from 2400 to 300 000 electrons with simulated noise for the simulation of real conditions, as is shown in Figure 5.17. This simulation shows the important outputs for pixel electronics verification, the CSA output, PDH output, and ANALOG_OUT.

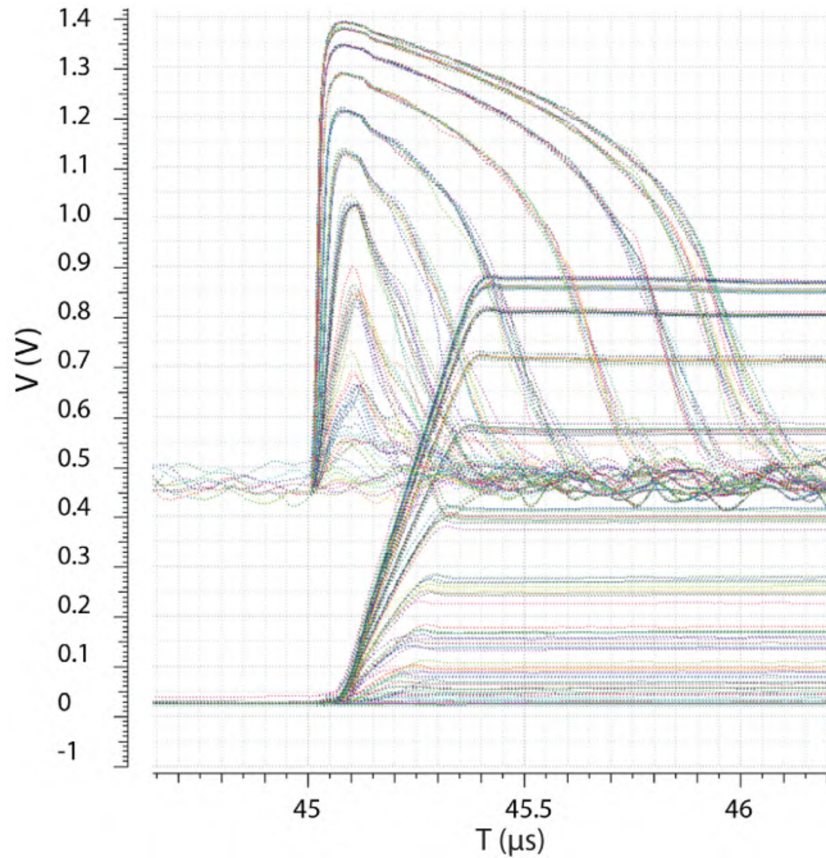



Figure 5.17: The simulation of the LORDS pixel electronics. The first curvers are the CSA output from 2400 $e^-$ to 300 000 $e^-$ and the second is the PDH output for the DAC input.

### 5.4.1 Low-Voltage Differential Signaling transmitter / receiver designed in 180 nm SOI technology

The main simulation test of the communication of the LORDS chip are the following chapter. The communication consists of two modes, the LVDS and CMOS mode. The architecture of LVDS drivers is based on the previous version in the X-CHIP-03, Figure 5.6. The eye diagram simulation of the LVDS communication is shown in Figure 5.19. The complexity fo the simulation consists of the input for the LVDS transmitter which is the row shift register. The maximum communication speed of the simulations, while the signal complies with the LVDS standard, is 480 MHz. The main modification of this design is widening of supply paths with respect to impedance for differential signal conduction,

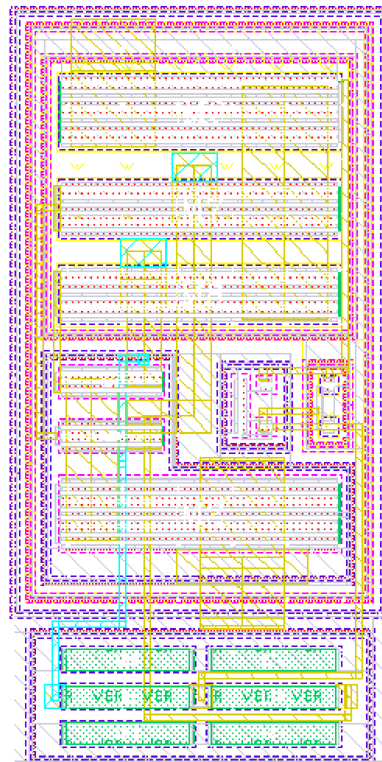


Figure 5.18: The LORDS LVDS transmitter layout in 180 nm SOI technology.

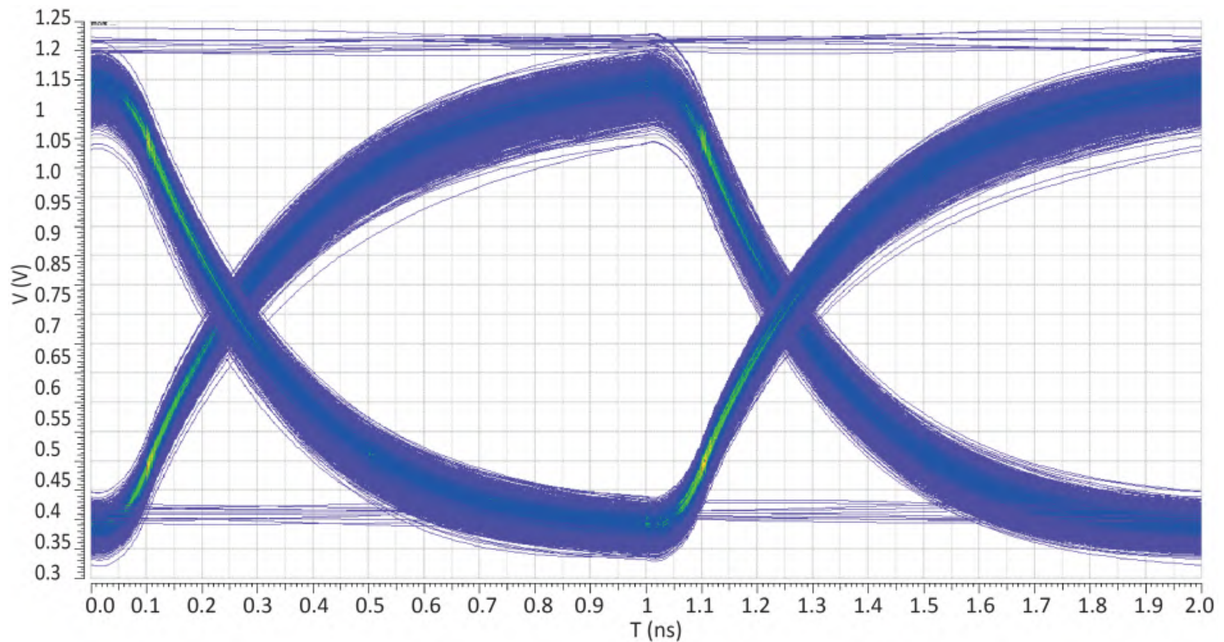



Figure 5.19: The LORDS eye diagram of the differential signal at 0.5 Gbps.

### 5.4.2 Summary of LORDS LVDS designed in the 180 nm CMOS technology

The LORDS design in 180 nm CMOS technology has been described. The pixels electronics and layout of the detector by the author has been done. The essential funckionality of this detector is the ADC mode, which is decribed by P. Vancura, T. Benka et al. in [89]. The LORDS prototype verified the electrical measurement of the LVDS drivers in the X-CHIP-03 in the simulations of the LVDS. The frequency of 200 MHz to 500 MHz in the simulation of complete communication with shift registers, with extracted parasitic capacitances and resistivities, has been increased by design modification in the layout. The immediate modification of LORDS detector improves the pixel design, which has an octagonal shape. The octonogal sensor has the main advantage in the density of the electric charge in the hanle-wafer. With the standard sensor design, the edges of the electric charge density are sharp during the simulation. One of the requirements of the sensor is the homogeneity of the magnetic field of adjacent sensors in the handle wafer, which the octagonal sensor can largely eliminate, section 5.4.

## 5.5 Test structures designed in 65 nm CMOS technology

Ultra deep submicron CMOS technologies provide enhanced radiation tolerance and possibility to integrate complex electronics in a small area, which makes them attractive for fabrication of pixel front-end chips. Presented work concerns the development of a charge injection circuit using 65 nm CMOS technology. This technology benefits from enhanced radiation tolerance and highly possibility to integrate highly complex electronics. The target application of this circuit is calibration of the pixel front-end chip that is being developed by the RD53 collaboration at CERN described by S. Marconi, M. B. Barbero, T. Benka et al. in [97] and [90] whose main task is the development of a new pixel chip for ATLAS [2] and CMS [3] experiments. Two prototype chips have been designed and manufactured. The first chip, subsection 5.5.1, contains a 12-bit VDAC and the second, subsection 5.5.2, implements the DAC in a charge injection circuit. The charge injection circuit consists of the following blocks: 12-bit VDAC, switch and analogue buffers. In addition, the second chip contains a charge sensitive amplifier and a bank of capacitors representing capacitive load of large pixel array that has been integrated for testing of the charge injection circuit. Design of both chips, as well as circuit simulations, laboratory measurements and studies of radiation tolerance are described.

### 5.5.1 Voltage DAC

The electronics block the VDAC formed the first prototype separately 5.20 which has been created in collaboration in collaboration with colleague M. Havránek. The first prototype consists of 10 channel of the VDACs for measurement the DAC voltage dispersion.

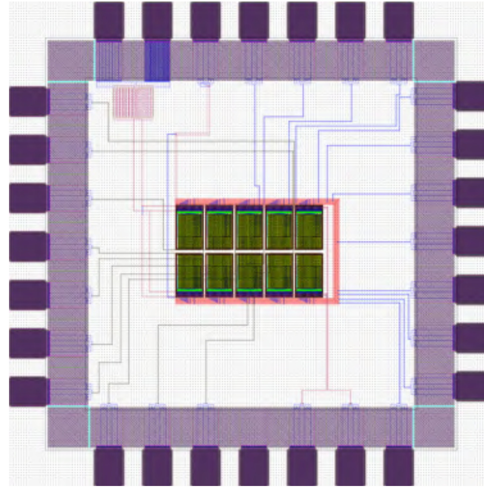


Figure 5.20: The first prototype of the VDAC layout designed in 65 nm CMOS technology. Inside the chips are 10 DACs for the voltage dispersion measurement.

Structure of 10-bit R-2R with 4-bit weighted ladder is included in the VDAC, as shown in Figure 5.21. Detailed schema of the switch in the VDAC is shown in Figure 5.22 The circuit has 12-bit resolution $\Rightarrow$ 4096 values $\Rightarrow$ 1 Least Significant Bit (LSB) $\approx$ 0.3 mV. The Low Voltage Threshold (LVT) transistors are used in the first prototype with transistors length 100 nm. The circuits powered by the VDAC require the Integral and Differential NonLinearities (INL and DNL) to be less than 5 LSB. The DNL in the simulation of the first prototype are smaller than 0.7 LSB and INL are smaller than 0.5 LSB.

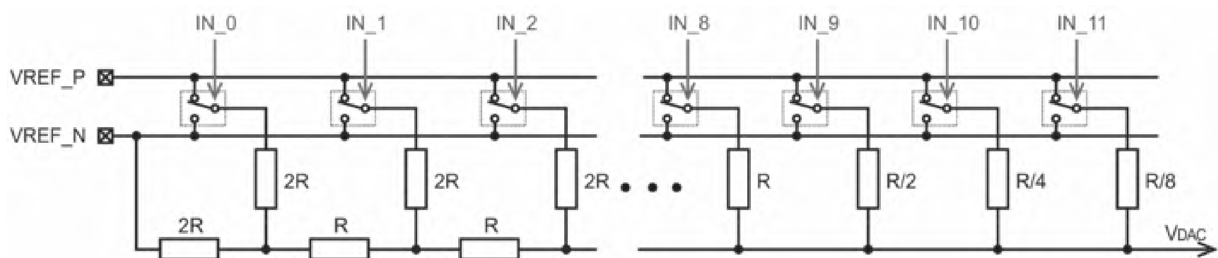



Figure 5.21: The DAC structure 10-bit R-2R with 4-bit weighted ladder.

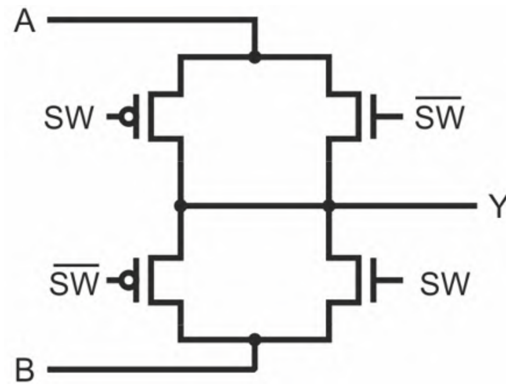



Figure 5.22: The switch schema of the the VDAC.

The electrical test measurement (before irradiation) of the INL and DNL are in Figures 5.23 and 5.24. The data are ploted for all 10 channels of the VDAC. The variance of data values are greater as before irradiation, the DNL 6 times and INL 40 times.

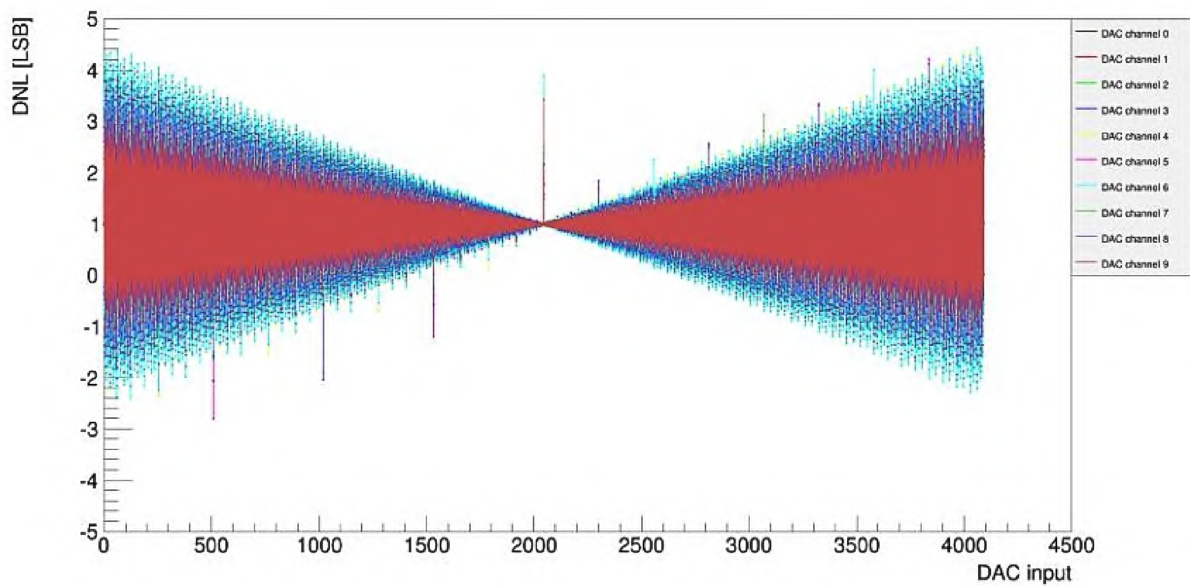



Figure 5.23: The DNL electrical measurement of the first prototype of the VDAC.

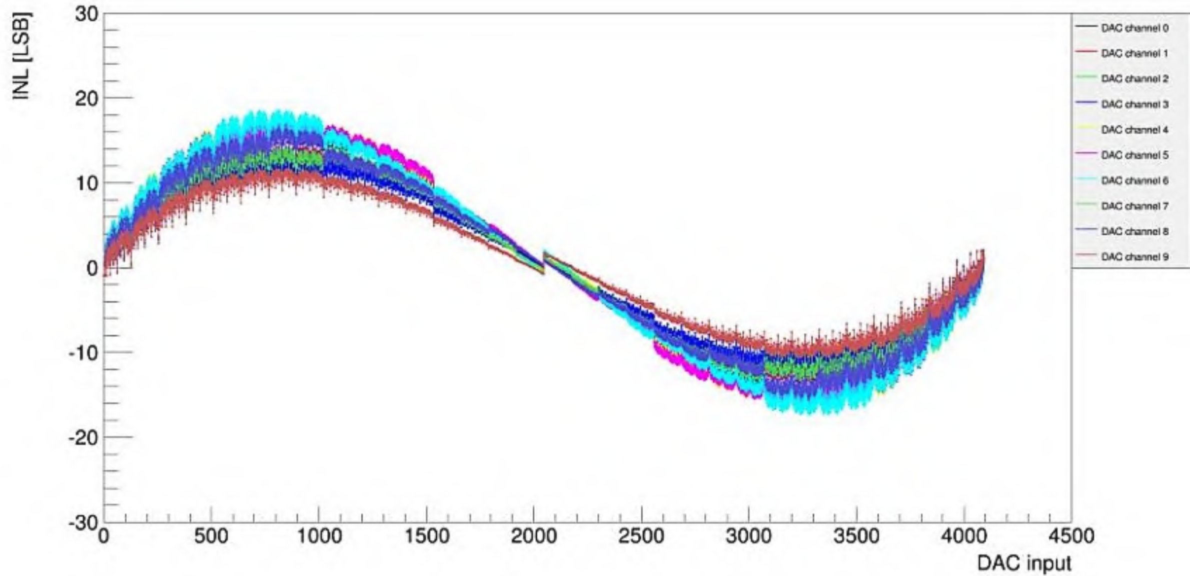



Figure 5.24: The INL electrical measurement of the first prototype of the VDAC.

As the radiation resistance of this block is high because it forms part of the pixel detector in the particle accelerator at CERN [90], two measurements with radioactive sources were performed. The first measurement represents $^{60}$Co radioactive source the Terabalt [98], 1.17 and 1.33 MeV with dose-rate 28 krad/min. Total dose of the fisrt prototype with $^{60}$Co is 100 Mrad in 59.5 hours. The difference between the measurements DNL and INL before and after irradiation is negligible, Figure 5.25 and Figure 5.26 shown the $^{60}$Co irradiation.

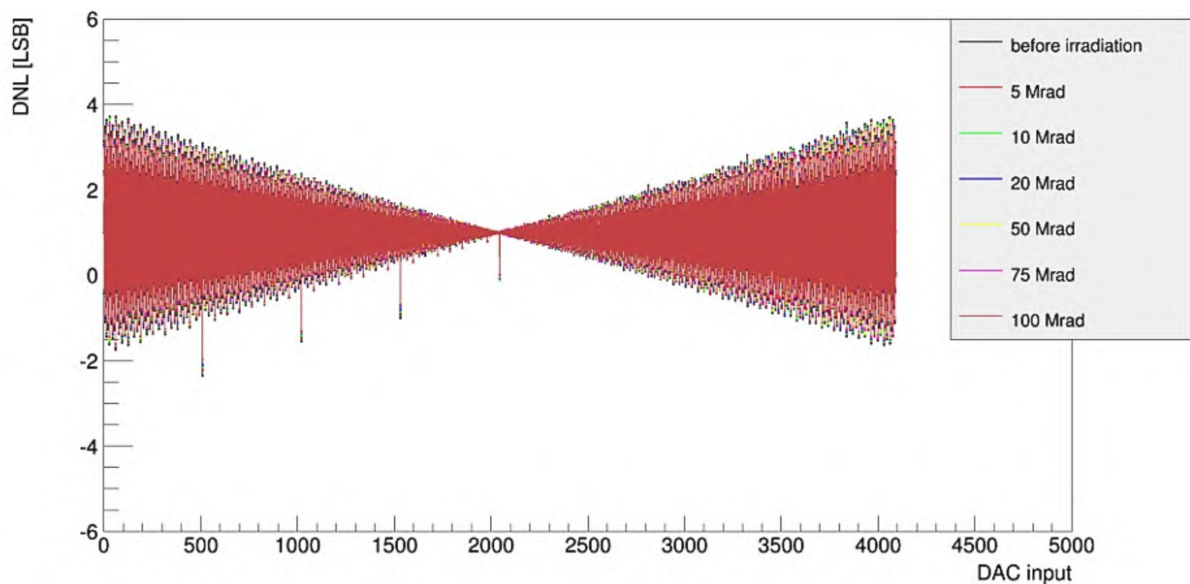



Figure 5.25: The DNL irradiation measurement of the first prototype with $^{60}$Co.

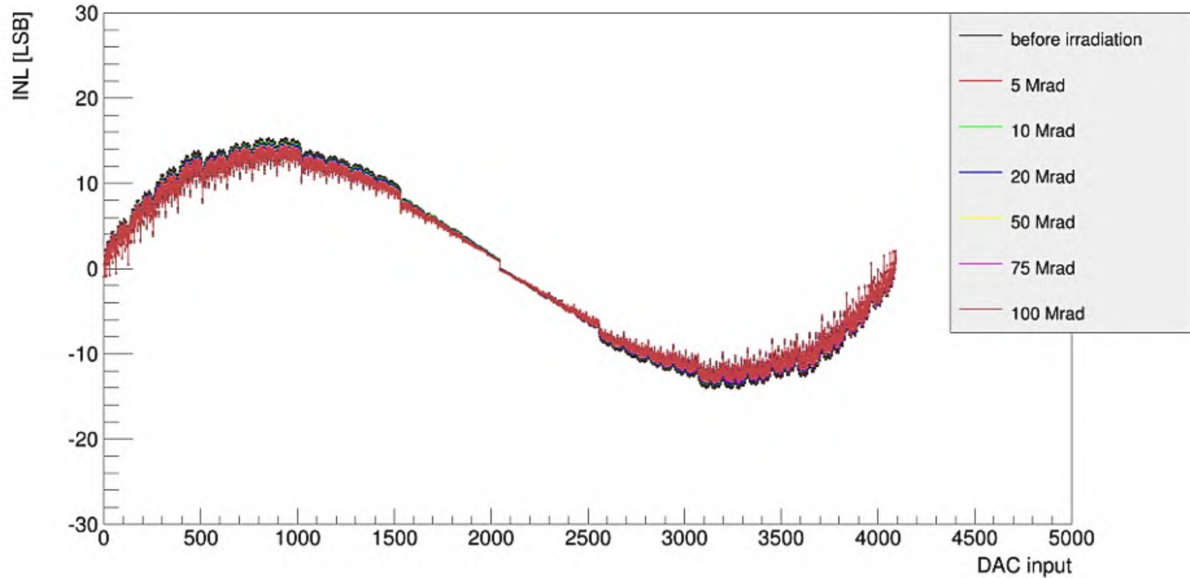



Figure 5.26: The INL irradiation measurement of the first prototype with $^{60}$Co.

The X-Ray tube - tungsten (W) targer, 50kV / 40 mA, forms the second irradiation measurement with dose-rate 7.8 Mrad/h, irradiation time 128.2 h and total dose rate is 1000 Mrad. The measurement with X-Ray source has an insignificant difference compared to the previous measurement with the $^{60}$Co source, Figure 5.27 and Figure 5.28.

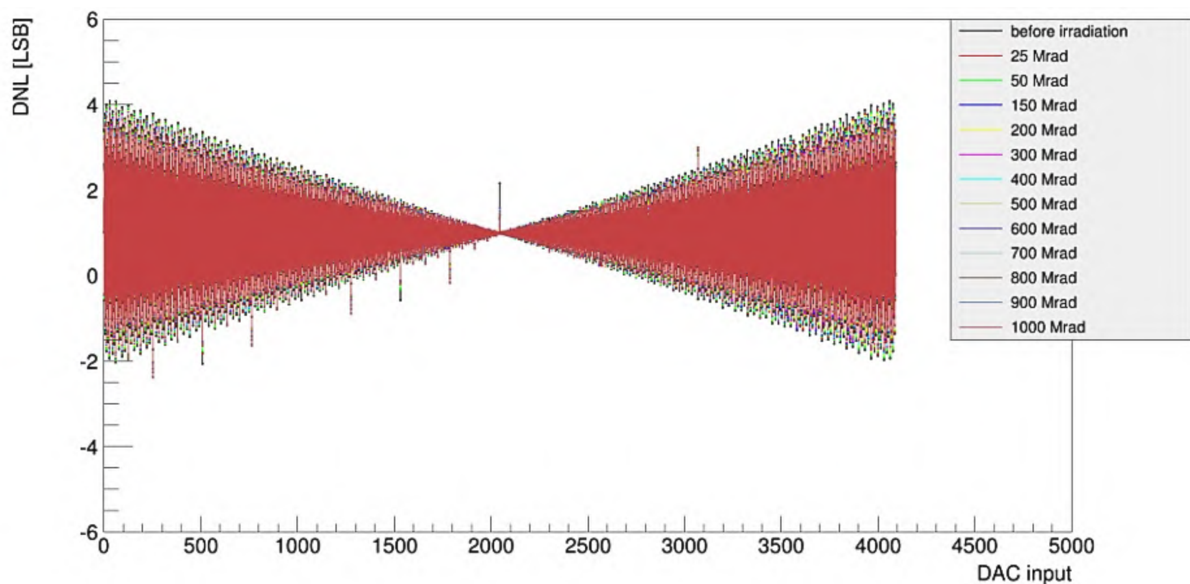



Figure 5.27: The DNL irradiation measurement of the first prototype with X-rays.

Comparation the simulations data with the electrical measurements before and after irradiotion results of the first prototype of the VDAC identifies an error in the design of microelectronic structures of the VDAC, despite performing a detailed design simulation in

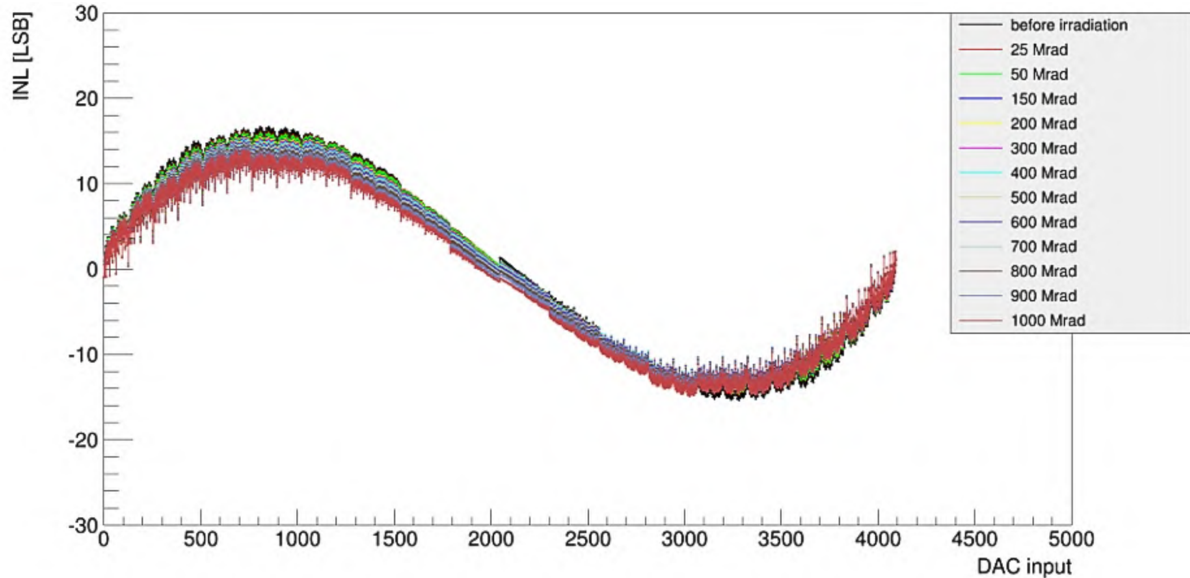



Figure 5.28: The INL irradiation measurement of the first prototype with X-rays.

defined irradiation conditions. Further study of the design and radiation damage showed that the VDAC output resistance increases by $\approx 12\%$ during irradiation. The reason is the insufficiently dimensioned power supply of the VDAC, which increased the irradiation resistance at VREF_P and VREF_N. The second reason is compliance with the minimum dimensions of the transistor length in the switches 5.22 (LVT NMOS: W/L = 2 $\mu$m / 100 nm; LVT PMOS: W/L = 6 $\mu$m / 100 nm). These results are not acceptable for the use of the block VDAC in the pixels detector of the RD53 collaboration; the second prototype with the necessary corrections is in the following chapter.

### 5.5.2 Charge injection circuit with voltage DAC

The revision of the previous version of VDAC and thus the correction of unacceptable results is implemented in the second prototype called INJECT_CHIP, Figure 5.29, has been developed and tested by the author. The increased resistivity of the power connection is eliminated by broadening the routing of VREF_P and VREF_N lines. The LVT transistors are replaced by standard transistors (STD) and their dimensions are as follows: (STD NMOS: W/L = 2 $\mu$m / 120 nm; STD PMOS: W/L = 6 $\mu$m / 120 nm). In the second prototype INJECT_CHIP is integrated the VDAC (first revision), CSA [99], Inject switch and three analog buffers, Figure 5.30.

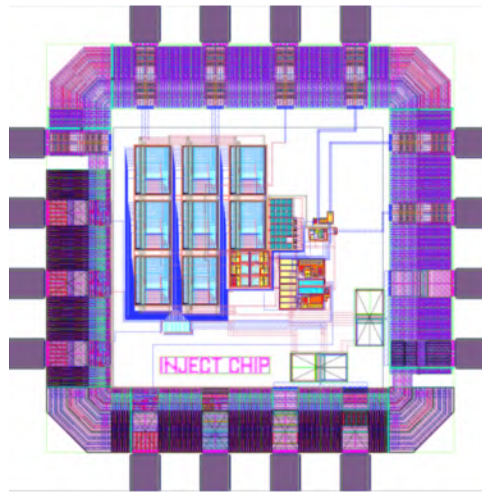



Figure 5.29: The layout of the INJECT_CHIP.

The primary goal of the INJECT_CHIP is to verify the functionality of VDACs with a load capacity of up to 2 pF to simulate the conditions used by the block in the RD53 pixel detector [90]. The INJECT_CHIP consists of 3 VDAC. Two of them are connected via a robust analog buffer to an injection switch that switches between the two voltage levels, INJECT_H and INJECT_L. The first analog buffer is designed for the upper half of the operating voltage, and the second for the lower half of the operating voltage for precision voltage inject. Two amplifiers buffer the VDAC levels (INJECT_H, INJECT_L) generated by the VDAC and are strong enough to drive capacitance load of 2 pF while preserving stability and reasonable slew rate.

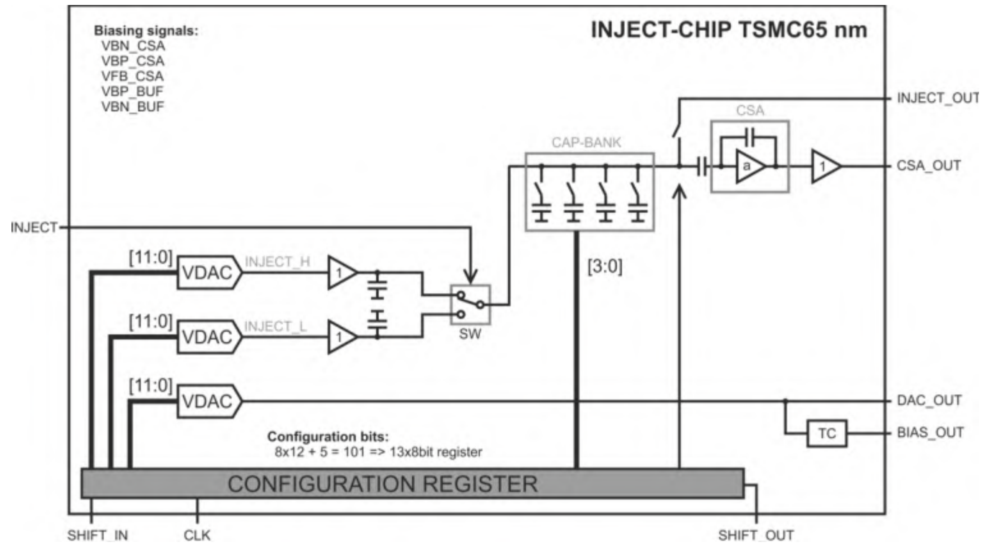



Figure 5.30: The block scheme of the INJECT_CHIP.

The architecture of the buffers is shown in Figure 5.31, the NMMOS unput diff-pair is in the AMP_H and the PMOS input diff-pair in the AMP_L. The closed loop gain is 2 for stability reasons and the open loop gain AMP_H is $\approx$ 4000 and AMP_L is $\approx$ 6500. Offset for both buffers is $<$ 1 mV at $\sigma \approx$ 1 mV (MC). The third VDAC is integrated in the chip for testing its linearity. A configurable array of capacitors with a maximum value of 2 pF @ 5 ns signal rise-time is connected between the inject switch and the CSA [99]. The output block consists of a CSA [99] with an analog buffer.

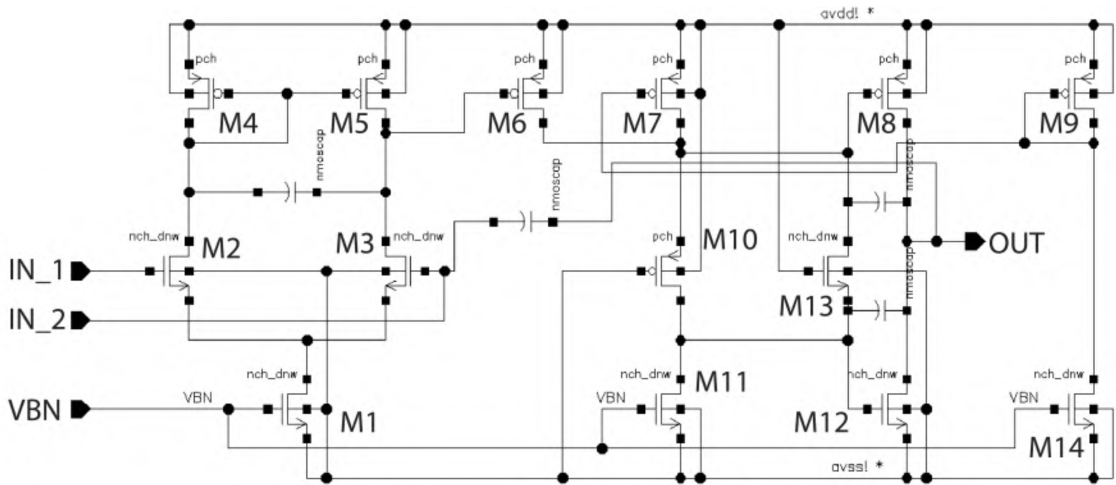



Figure 5.31: The scheme of the voltage buffer (AMP_H) of the INJECT_CHIP.

The nonlinearities in the simulation are smaller than 0.3 LSB. The electrical test measurement (before irradiation) of the INL and DNL are in Figures 5.32 and 5.33. The DNLs are approximately the same when comparing simulation and electrical measurement as the first prototype. Individual peaks represent a transient phenomenon of switching separate switches in the 12- bit VDAC. These peaks do not affect the functionality of the VDAC because the voltage value is set during the chip configuration and does not not during its operation. The INLs are 10 times higher than in the simulation. The results of the electrical measurements of DNLs and INLs are acceptable for the RD53 collaboration [90].

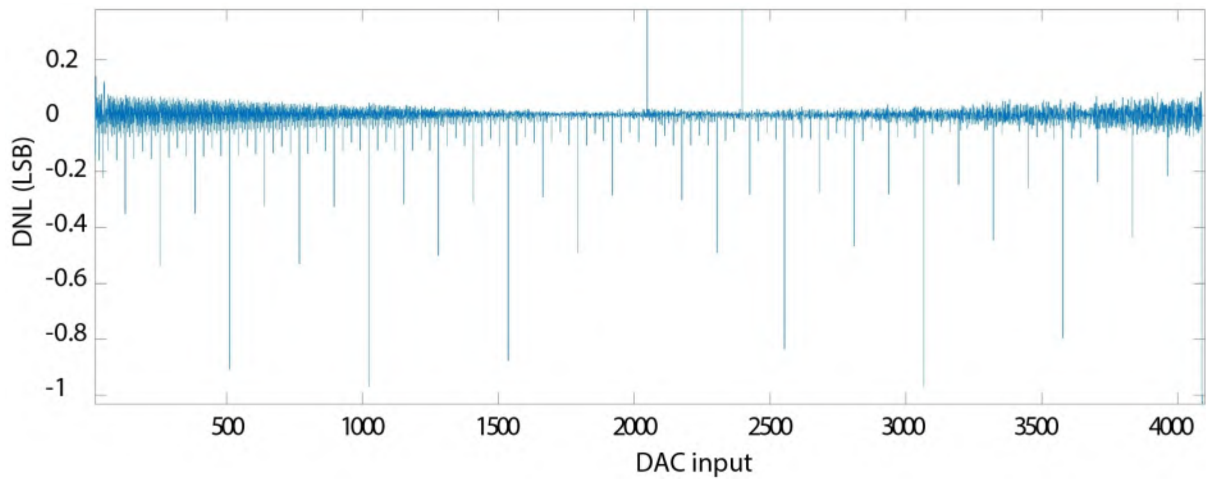



Figure 5.32: The DNL electrical measurement of the second prototype the INJECT_CHIP VDAC.

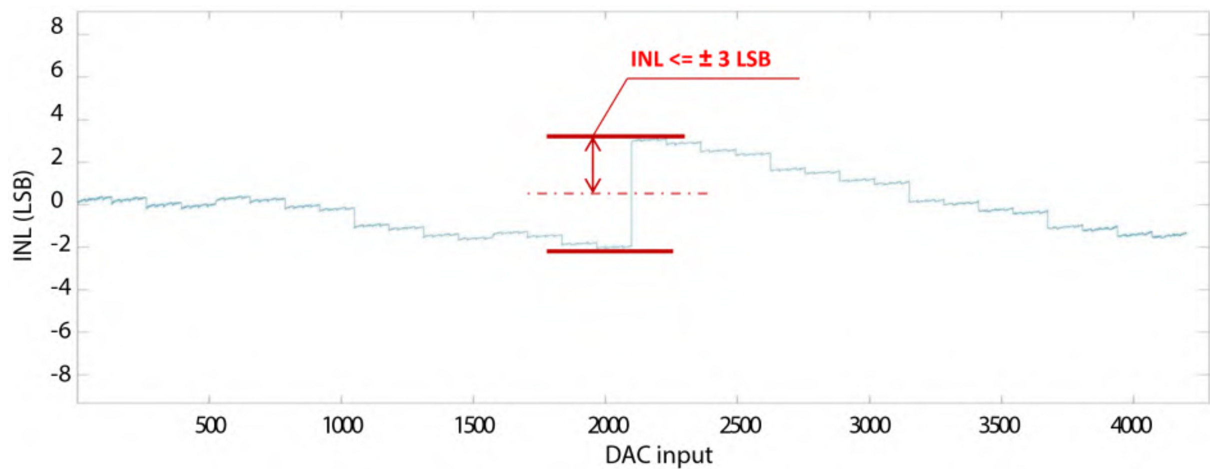



Figure 5.33: The INL electrical measurement of the second prototype the INJECT_CHIP VDAC.

The INJECT signal of the Figure 5.30 left is set to 200 kHz to simulate a signal from a pixel sensor, Figure 5.34. In the Figure 5.35 is shown the transmission characteristic of the rise and fall edge as the output of INJECT_OUT, Figure 5.30 right.

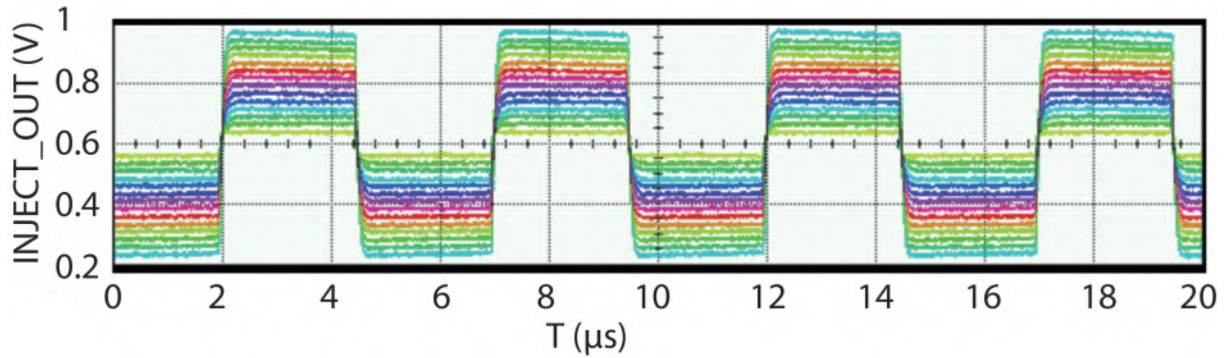



Figure 5.34: The electrical measurement of the INJECT_CHIP. The measured output is the INJECT_OUT; INJECT = 200 kHz @ 2 pF.

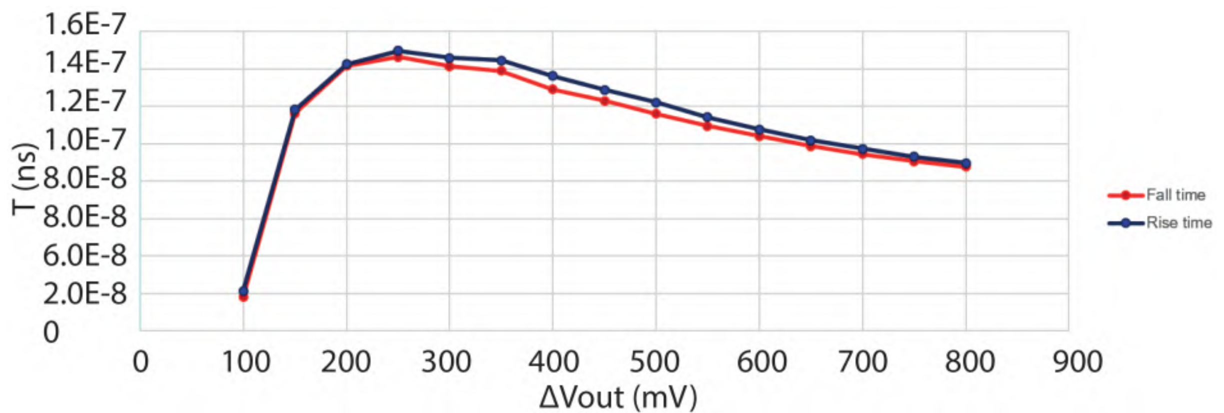



Figure 5.35: The rise and fall time of the INJECT_OUT of the INJECT_CHIP at INJECT = 200 kHz @ 2 pF.

The Charge sensitive amplifier output, Figure 5.30 right, with the Inject (voltage levels from DACs) from 100 mV to 700 mV and with 50 mV step is shown in Figure 5.36. The threshold of the pulse length measurement is 50 mV (TOT), Figure 5.37.

The measurement with a radiation sources was only possible with an X-ray source (100 kV @ 30 mA, 5.07 Mrad/h) and the total radiation absorbed dose is 870 Mrad due to X-rays malfunction. The measured data after irradiation of the DNLs and INLs are shown on Figure 5.38 and 5.39. The result of the X-rays measurement at 870 Mrad is that the second prototype the first revision of the VDAC is completely acceptable and deficiencies from the previous version have been eliminated. The testing blocks for the VDAC as the Inject switch, capacitors array, and Charge sensitive amplifier enabled verification and validation of the developed microelectronic structure of the VDAC. The RD53 pixel detector was submitted, manufactured and used in many experiments at CERN with the second prototype of the VDAC.

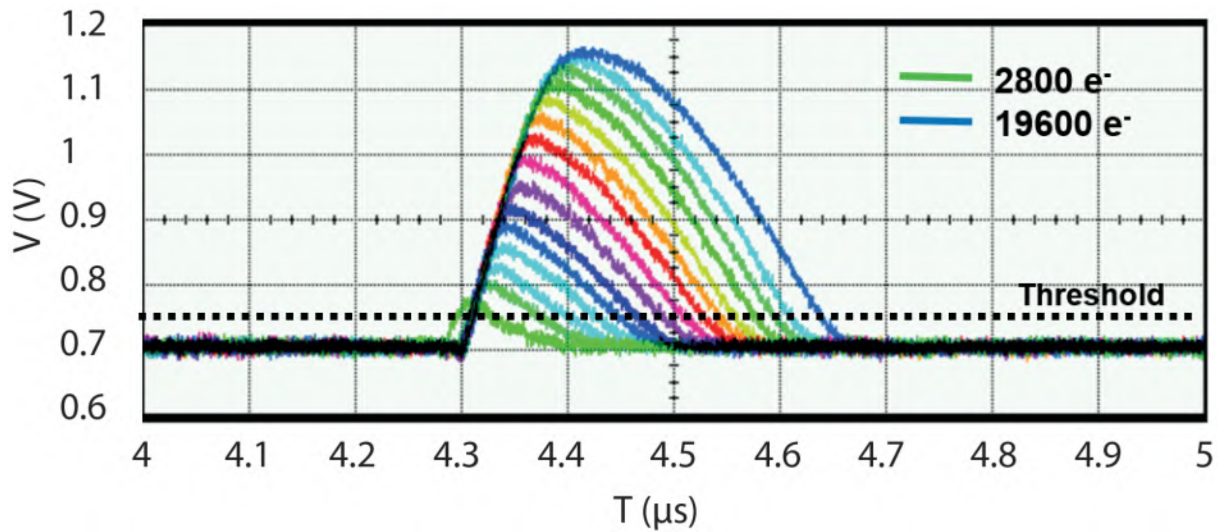



Figure 5.36: The electrical measurement of the INJECT_CHIP. The measured output is the CSA_OUT; VDACs inject is from 100 mV to 700 mV with 50 mV step. The smallest curve corresponds to 2800 $e^-$ and the highest to 19.600 $e^-$.

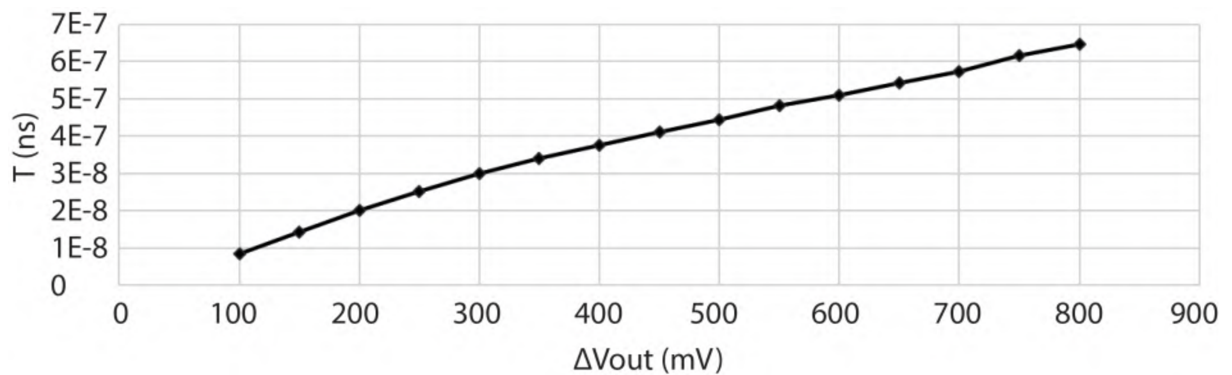



Figure 5.37: Characterization the time over threshold of the Charge sensitive amplifier; CSA_OUT; the threshold of the pulse length measurement is 50 mV (TOT).

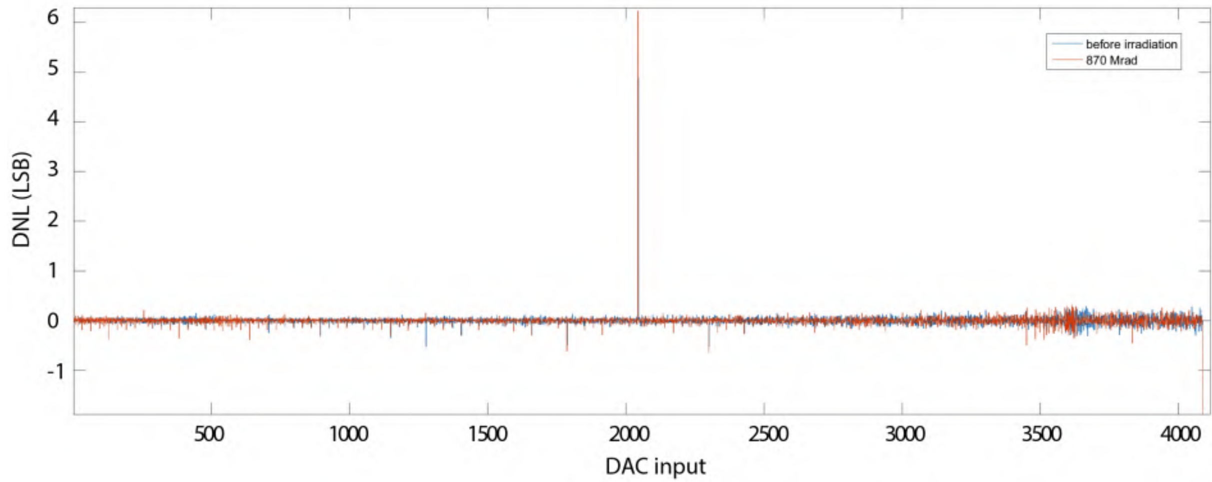



Figure 5.38: The DNL irradiation measurement of the second prototype INJECT_CHIP with X-rays up to 870 Mrad.

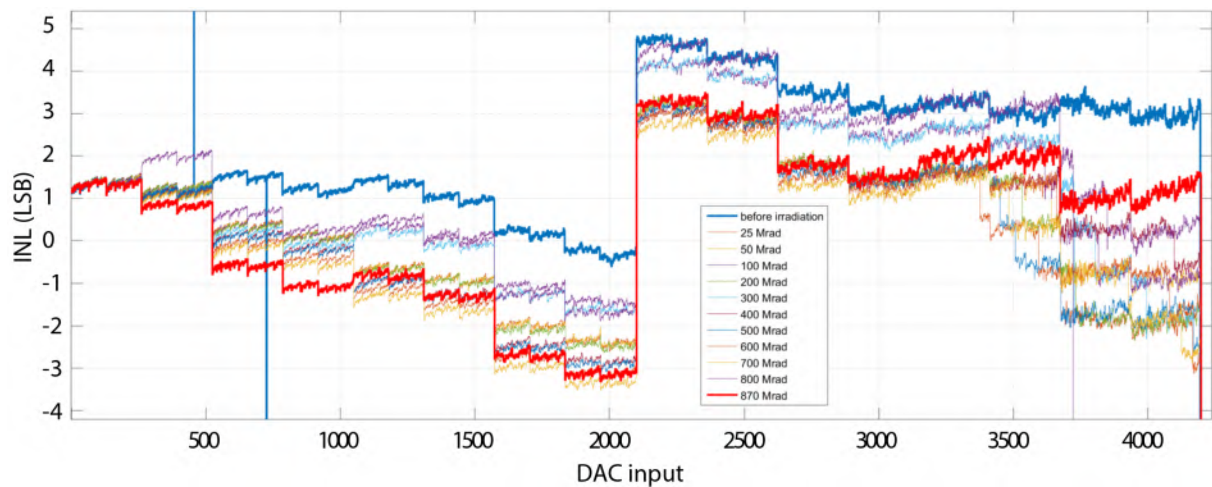



Figure 5.39: The INL irradiation measurement of the second prototype INJECT_CHIP with X-rays up to 870 Mrad.

### 5.5.3 Summary of blocks designed in 65 nm CMOS technology

Two prototype chips have been designed and manufactured. The first chip contains a 12-bit VDAC and the second implements the DAC in a charge injection circuit. The first prototype for radiation resistance up to 100 Mrad with $^{60}$Co and X-rays has been tested. The characteristics of INL and DNL do not meet the requirements for radiation requirements. The second prototype was irradiated only by X-rays. It turned out that the comparison of $^{60}$Co and X-rays measurements of the first prototype is almost identical. The X-rays irradiation of the second prototype is sufficient, but to determine the damage of the device, a measurement of up to 870 Mrad has been performed. The change in properties at 870 Mrad is not significant; we can assume radiation resistance up to 1000 Mrad. The charge injection circuit consists of the following blocks: 12-bit VDAC, switch and analogue buffers. Design of both chips, as well as circuit simulations, laboratory measurements and studies of radiation tolerance were described. The most crucial characterization and measurements consisted of creating INL and DNL measurements during irradiation. The first prototype did not meet the expected requirements, but INL = $\pm$3 LSB and DNL = $\pm$0.2 LSB forms the second prototype, which is acceptable for the subsequent implementation of the block into the detector of the RD53 collaboration at CERN, development and functionaly and development is descibed by author in [97] and [90].

# Chapter 6

# Conclusion

The presented dissertation study was created to show the current state of research which is represented by the imaging detector X-CHIP-02, its continued prototype versions and essential microelectronics test blocks in various technologies for characterization for continuing and, therefore, future development of pixels detectors designed in 180 nm SOI CMOS technology. Specifically, this study focuses on the development of the pixel detector X-CHIP-02 which is manufactured in deep submicron 180 nm SOI CMOS technology. Basic parameters and important blocks of the X-CHIP-02, as well as the latest results, were described. Knowledge and experience with pixel detectors were obtained during solving the research project and grants that were solved at the Department of Microelectronics FEE CTU and at the Department of Physics FNSPE CTU in Prague. The proposals of the chip have been developed in cooperation with Advanced Detection Systems of Ionizing Radiation Project at the FNSPE CTU in Prague.

The presented study was conducted to better understand the behavior of sensitive elements of the developed SOI MAPS sensor. Fundamental parameters and characterization of the test structure of the X-CHIP-02, as well as the latest results, were described in[19] by the author. To achieve acceptable detector sensitivity, a high quality Si-$SiO_2$ interface between the BOX layer and the handle wafer (substrate) must be ensured. An undesirable effect of the trapped positive charge has been observed during irradiation in the Si-$SiO_2$ interface. The IV characteristics during the X-rays irradiation without shielding (Figure 4.38) show the increasing level of the trapped positive charge. If the X-ray source is turned off, the sensor current decreases exponentially by 10 - 15 % in an hour. After 1 hour $\pm$ 10 minutes, the sensor current is stabilized. The stabilization time is affected by the setup settings, technological variations of the chip, X-ray source, etc. The trapped positive charge is proved that the measurement with lead shielding and a pinhole in the HV bias ring area of the detector. The appropriate solution to eliminate this effect is the use of technological process P-STOP and P-SPRAY, as is described in [81].

All the relevant circuit blocks of both pixel matrices were presented here. The ultimate goal of pixel types fo X-CHIP-02 is pixel with 50 $\mu$m pixel pitch, which has a small capacitance (2.9 $\pm$ 0.1 fF by -100 V), relatively little noise, low leakage current (well below 1 $\mu$A at -100 V) and appropriate HV bias ring. The pixel matrix with a 100 $\mu$m pixel pitch was not used for imaging, since many pixels have high noise, descibed by M. Havranek, T. Benka et al. in [23]. The capacitance of the sensor diodes, simulated in the TCAD, is higher due to ideal parameters of the silicon structure and the parasitic capacitances of the test structure, which have not been included into the simulation model. An important section describing the radiation damage of the chip contains transistor structure with $^{60}$Co ionization damage and results from the X-rays and the TEM.

The second the X-CHIP-03 prototype of pixels detector contains a single pixel matrix with 50 $\mu$m pixel pitch. Single-ended communication is not possible for large-scale detector communication due to insufficient data throughput; therefore, this prototype was designed to validate and verify a new communication architecture, which represents the Low-Voltage Differential Signaling (LVDS) drivers. The first microelectronics cirtuis of the LVDS was designed in 150 nm CMOS technology and the architecture for the X-CHIP-03 has been used. The necessary simulation and electrical measurements are contained in subsection 5.3.1. The maximum frequency 200 MHz Was verified for successful differential communication due to narrow metalizations paths of the supply power in the layout and impedance mismatch. The LORDS prototype verified the electrical measurement of the LVDS drivers in the X-CHIP-03 in the simulations of the LVDS. The frequency of 200 MHz to 500 MHz in the simulation of complete communication with shift registers, with extracted parasitic capacitances and resistivities, has been increased by design modification in the layout. The immediate modification of LORDS detector improves the pixel design, which has an octagonal shape. The octonogal sensor has the main advantage in the density of the electric charge in the hanle-wafer. With the standard sensor design, the edges of the electric charge density are sharp during the simulation. One of the requirements of the sensor is the homogeneity of the magnetic field of adjacent sensors in the handle wafer, which the octagonal sensor can largely eliminate, section 5.4.

Development of a novel pixel detector in SOI CMOS technology is still a challenge. Various experiments have performed to demonstrate the proper functionality of the X-CHIP-02, X-CHIP-02-PCB, SURE and X-CHIP-03 and LORDS. The contribution of present and future research is in the development of the new pixel detector in 180 nm SOI CMOS technology for specific applications in the industry. Concerning the application in X-ray imaging, the capability of operating a monolithic pixel detector in partially depleted mode gives numerous advantages [100]–[103]. For minimum ionizing particles it means maximizing the charge collection, leading to a higher signal to noise

ratio and radiation tolerance.

Ultra deep submicron CMOS technologies provide enhanced radiation tolerance and possibility to integrate complex electronics in a small area, which makes them attractive for fabrication of pixel front-end chips. Presented work concerns the development of a charge injection circuit using 65 nm CMOS technology. This technology benefits from enhanced radiation tolerance and highly possibility to integrate highly complex electronics. The target application of this circuit is calibration of the pixel front-end chip that is being developed by the RD53 collaboration at CERN described by S. Marconi, M. B. Barbero, T. Benka et al. in [97] and [90] whose main task is the development of a new pixel chip for ATLAS [2] and CMS [3] experiments. Two prototype chips have been designed and submitted. The first chip contains a 12-bit VDAC and the second implements the DAC in a charge injection circuit. The charge injection circuit consists of the following blocks: 12-bit VDAC, switch and analogue buffers. Design of both chips, as well as circuit simulations, laboratory measurements and studies of radiation tolerance were described. The most crucial characterization and measurements consisted of creating INL and DNL measurements during irradiation. The first prototype did not meet the expected requirements, but INL = ±3 LSB and DNL = ±0.2 LSB forms the second prototype, which is acceptable for the subsequent implementation of the block into the detector of the RD53 collaboration at CERN, development and functionaly and development is descibed by the author in [97] and [90].

## 6.1 Summary of thesis

Semiconductor radiation detectors play a crucial role in experimental particle physics, mainly due to their spatial resolution, relatively large signal, and radiation resistance. Their use is mainly in orbital detectors of complex experiments, such as the ATLAS experiment in the CERN particle laboratory in Switzerland. The application of pixel detectors has significant overlap in several practical applications. The department at the FNSPE CTU is engaged in developing a sensor for radiation imaging designed in SOI CMOS 180 nm technology. This technology represents a competitive field of pixel detectors compared to other manufacturing technologies, especially hybrid pixel detectors. Semiconductor detection systems have several practical applications and go far beyond the scientific sphere. Examples are the radiation imaging, defectoscopy, or dosimetry. The parameters of the detectors are strongly dependent on the technologies of the production of sensors and read-out chips. The rapid development of technologies for the production of integrated circuits allows the implementation of a new solution that could not be implemented with previous technologies.

Various technologies are used for the production of ionizing pixel detectors. Hybrid pixel detectors include one of the most widely used ionizing radiation detector technologies. These are the various technologies used in manufacturing the front-end chip, sensor, and the interconnection between the chip and the sensor, which is reflected in the high cost and complexity of manufacture. The SOI technology is a comprehensive solution in which the sensor and front-end electronics are implemented in a single design (handling wafer). This feature of SOI enables competition with hybrid detectors and creates a new area of research in academia and industry.

The prototype of the X-CHIP-02 was successfully tested in industrial facilities, and its parameters are better than just acceptable. The second prototype, the X-CHIP-03 and LORDS, is presented as the first final versions for series production. Many microelectronic blocks in the prototypes are unsatisfactory, and therefore a partial or complex modification of the individual blocks is required. The prototype contains unsuitable microelectronic structures for communication with sensors in many applications. The processing of large amounts of data and the speed with which they are read takes advantage of the need to use LVDS communication. The follow-up project includes one of the essential parts of communication - acquiring and writing detector data.

Participation and cooperation in the RD53 group (CERN) includes a unique project that combines the three most extensive experiments in the international organization CERN, namely ATLAS [2], CMS [3] and ALICE [4]. The international project aims to develop new reading chips in the advanced depth-submicron popular 65 nm technology for the detection of ionizing radiation. The perspective of the follow-up project is to participate in the testing of the said complex chip the development of possible modifications or new structures in the 65 nm technology.

## 6.2 Fulfilments of targets

The presented study was created to show the current state of research which is represented by the imaging detector X-CHIP-02. Specifically, this study focuses on the development of the pixel detector X-CHIP-02 which is manufactured in ultra-deep submicron 180 nm SOI CMOS technology. Basic parameters and important blocks of the X-CHIP-02, as well as the latest results, were described. Knowledge and experience with pixel detectors were obtained during solving the research project and grants that were solved at the Department of Microelectronics FEE CTU and at the Department of Physics FNSPE CTU in Prague. The proposals of the chip have been developed in cooperation with Advanced Detection Systems of Ionizing Radiation Project at the FNSPE CTU in Prague. All the relevant circuit blocks of both pixel matrices were presented here. The 100 $\mu$m

pixel matrix was not used for imaging, since many pixels have a high noise. An important section describing the radiation damage of the chip contains transistor structure with $^{60}$Co ionization damage and results from the X-rays and the TEM. Development of a new pixel detector in SOI CMOS technology is still a challenge. Various experiments have performed to demonstrate the proper functionality of the X-CHIP-02, X-CHIP-02-PCB and SURE.

The contribution of present and future research is in the development of the new pixel detector in 180 nm SOI CMOS technology for specific applications in the industry. The personal contribution of the author to the disertation are following:

- Design, implementation and electrical measurement of the X-CHIP-02 pixels detector 180 nm SOI CMOS technology. Functionality verification of the X-CHIP-02 with the TEM, $^{60}$Co and X-rays, characterization of the test structure of the X-CHIP-02 during irradiation. Evaluation and derivation of the conclusions from the radiation damage of microelectronic structures in the detector in 180 nm SOI CMOS technology.

- Development of the second prototype of the X-CHIP-02 pixel detector in 180 nm SOI CMOS technology the X-CHIP-03 with LVDS drivers for the high speed communication. The verification of the LVDS blocks with electrical measurements and the development of a second prototype with eliminated unacceptable features.

- Development of the thirds prototype of the X-CHIP-02 pixel detector in 180 nm SOI CMOS technology the LORDS octagonal pixels detertor for LEO with required parameters of this detector for the purpose of its use. The LVDS drivers modification for the large - scale detectors.

- Development, implementation, electrical measurement and radiation tests at 1000 Mrad in the 65 nm technology the voltage Digital-to-analog converter with the appropriate circuits to perform the radiation tests. The first prototype of the SOI modifications for the acceptable radiation resistance requirements that are implemented in the second prototype, the INJECT_CHIP.

This dissertation has not implemented the following points of interest in testing microelectronic structures due to the participation of other projects:

- Electrical and radiation measurements of the pixels electronics with the X-CHIP-03 and LORDS detectors, although the architecture is identical to the slight modifications to X-CHIP-03.

## 6.3 Further extensibility and recommendations

The proposed microelectronic structures in 180 nm technology in cooperation with the Department of Physics, FNSPE CTU were used for read-out read chip, which is used in strip detectors of ionizing radiation and will be used slight modifications in the industry. The pixel detector in SOI technology creates a new competitive area in the industrial and scientific market. The first prototype, X-CHIP-02, was successfully tested in industrial facilities, and its parameters are better than just acceptable. The second prototype, X-CHIP-03 and LORDS, as the first final version for series production have been manufactured. The first prototype, X-CHIP-02, contains non-compliant microelectronic structures for communication with the sensor in many applications. The processing of a large amount of data and their reading speed makes it necessary to use high-speed communication using LVDS. The LORDS detector due to its range of charge sensitive amplifier and radiation resistance has the advantage of standard architectures in space applications such as particle identification and dosimetry. Follow-up projects, included in this work, implement one of the essential parts of communication - the acquisition and recording detector data. Many microelectronic blocks in the prototypes are unsatisfactory, and therefore a partial or complex modification of individual blocks is necessary, which was performed in subsequent prototypes and are used for research activities and form the basis for future series production of pixel detectors designed in SOI CMOS technology.

The development of microelectronic structures in two prototypes in ultra-deep submicron 65 nm CMOS technology has the main result of establishing cooperation with the vital organization CERN and their available technologies to investigate radiation resistance. For future cooperation, it is recommended to continue to participate in the development of detectors in deep-submicrons technologies and have at their disposal technologically unique equipment for testing and finding the application of microelectronic structures.

# Appendix A

# List of candidate's work related to the thesis

The percentage is even for all listed authors at each publication. The second indent represents the citations of the article.

## Journals (Impact)

- T. Benka, M. Havranek, M. Hejtmanek, *et al.*, "Characterization of pixel sensor designed in 180 nm SOI CMOS technology", *JOURNAL OF INSTRUMENTATION*, vol. 13, 2018, 19th International Workshop on Radiation Imaging Detectors (IWORID), AGH Univ Sci & Technol, Krakow, POLAND, JUL 02-06, 2017, ISSN: 1748-0221. DOI: `10.1088/1748-0221/13/01/C01025`
  - M. Havranek, T. Benka, M. Hejtmanek, *et al.*, "MAPS sensor for radiation imaging designed in 180 nm SOI CMOS technology", *JOURNAL OF INSTRUMENTATION*, vol. 13, 2018, 19th International Workshop on Radiation Imaging Detectors (IWORID), AGH Univ Sci & Technol, Krakow, POLAND, JUL 02-06, 2017, ISSN: 1748-0221. DOI: `10.1088/1748-0221/13/06/C06004`
- P. Vancura, M. Havranek, T. Benka, *et al.*, "A capacitor dac for charge redistribution analog to digital converter with successive approximation", cited By 1, vol. 343, 2018
  - M. Havranek, T. Benka, M. Hejtmanek, *et al.*, "X-CHIP-03: SOI MAPS radiation sensor with hit-counting and ADC mode", in *2018 IEEE NUCLEAR SCIENCE SYMPOSIUM AND MEDICAL IMAGING CONFERENCE PROCEEDINGS (NSS/MIC)*, IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Sydney, AUSTRALIA, NOV 10-17, 2018, IEEE Nucl & Plasma Sci Soc; IEEE, 2018, ISBN: 978-1-5386-8494-8

- L. Gaioni, M. B. Barbero, T. Benka, *et al.*, "Test results and prospects for RD53A, a large scale 65 nm CMOS chip for pixel readout at the HL-LHC", *NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH*, vol. 936, 282–285, 2019, ISSN: 0168-9002. DOI: `10.1016/j.nima.2018.11.107`

  - D. Ruini and C. T. Grp, "Serial powering and high hit rate efficiency measurement for the Phase 2 Upgrade of the CMS Pixel Detector", *JOURNAL OF INSTRUMENTATION*, vol. 14, 2019, 9th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (PIXEL), Activ Ctr Acad Sinica, Taipei, TAIWAN, DEC 10-14, 2018, ISSN: 1748-0221. DOI: `10.1088/1748-0221/14/10/C10024`

  - L. Gaioni, M. Manghisoni, L. Ratti, *et al.*, "Optimization of the 65-nm CMOS Linear Front-End Circuit for the CMS Pixel Readout at the HL-LHC", *IEEE TRANSACTIONS ON NUCLEAR SCIENCE*, vol. 68, no. 11, 2682–2692, 2021, ISSN: 0018-9499. DOI: `10.1109/TNS.2021.3117666`

  - M. Daas, Y. Dieter, J. Dingfelder, *et al.*, "BDAQ53, a versatile pixel detector readout and test system for the ATLAS and CMS HL-LHC upgrades", *NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH SECTION A-ACCELERATORS SPECTROMETERS DETECTORS AND ASSOCIATED EQUIPMENT*, vol. 986, 2021, ISSN: 0168-9002. DOI: `10.1016/j.nima.2020.164721`

  - S. Orfanelli and C. Collaboration, "The Phase 2 Upgrade of the CMS Inner Tracker", *NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH*, vol. 980, 2020, ISSN: 0168-9002. DOI: `10.1016/j.nima.2020.164396`

  - V. Perovic and C. T. Grp, "Serial powering in four-chip prototype RD53A modules for Phase 2 upgrade of the CMS pixel detector", *NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH*, vol. 978, 2020, ISSN: 0168-9002. DOI: `10.1016/j.nima.2020.164436`

  - L. Gaioni, M. Manghisoni, L. Ratti, *et al.*, "Threshold tuning DACs for pixel readout chips at the High Luminosity LHC", *NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH*, vol. 969, 2020, ISSN: 0168-9002. DOI: `10.1016/j.nima.2020.164025`

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(PIXEL), Activ Ctr Acad Sinica, Taipei, TAIWAN, DEC 10-14, 2018, ISSN: 1748-0221. DOI: `10.1088/1748-0221/14/10/C10017`

- Z. Janoska, T. Benka, M. Havranek, *et al.*, "Time of flight measurements with the PH32 chip", *JOURNAL OF INSTRUMENTATION*, vol. 14, 2019, 20th International Workshop on Radiation Imaging Detectors, Sundsvall, SWEDEN, JUN 24-28, 2018, ISSN: 1748-0221. DOI: `10.1088/1748-0221/14/04/C04004`
  - P. Vancura, M. Havranek, and J. Jakovenko, "Improvement of column-parallel sampling for a monolithic pixel detector", *JOURNAL OF INSTRUMENTATION*, vol. 15, no. 2, 2020, ISSN: 1748-0221. DOI: `10.1088/1748-0221/15/02/P02014`
- M. Marcisovska, T. Benka, M. Havranek, *et al.*, "A comparative study of the TID radiation effects on ASICs manufactured in 180 nm commercial technologies", *JOURNAL OF INSTRUMENTATION*, vol. 13, 2018, 20th International Workshop on Radiation Imaging Detectors, Sundsvall, SWEDEN, JUN 24-28, 2018, ISSN: 1748-0221. DOI: `10.1088/1748-0221/13/12/C12003`
  - M. Marcisovska, D. Dudas, M. Havranek, *et al.*, "TID and SEU testing of the novel X-CHIP-03 monolithic pixel detector", *JOURNAL OF INSTRUMENTATION*, vol. 15, no. 1, 2020, 21st International Workshop on Radiation Imaging Detectors, Crete, GREECE, JUL 07-12, 2019, ISSN: 1748-0221. DOI: `10.1088/1748-0221/15/01/C01043`
  - V. Vrba, T. Benka, J. Fojtik, *et al.*, "The SpacePix-D radiation monitor technology demonstrator", *JOURNAL OF INSTRUMENTATION*, vol. 13, 2018, 20th International Workshop on Radiation Imaging Detectors, Sundsvall, SWEDEN, JUN 24-28, 2018, ISSN: 1748-0221. DOI: `10.1088/1748-0221/13/12/C12017`
  - M. Marcisovska, T. Benka, M. Finger, *et al.*, "A study of single event effects induced by heavy charged particles in 180 nm SoI technology", in *2018 IEEE NUCLEAR SCIENCE SYMPOSIUM AND MEDICAL IMAGING CONFERENCE PROCEEDINGS (NSS/MIC)*, IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Sydney, AUSTRALIA, NOV 10-17, 2018, IEEE Nucl & Plasma Sci Soc; IEEE, 2018, ISBN: 978-1-5386-8494-8
- V. Vrba, T. Benka, J. Fojtik, *et al.*, "The SpacePix-D radiation monitor technology demonstrator", *JOURNAL OF INSTRUMENTATION*, vol. 13, 2018, 20th International Workshop on Radiation Imaging Detectors, Sundsvall, SWEDEN, JUN 24-28, 2018, ISSN: 1748-0221. DOI: `10.1088/1748-0221/13/12/C12017`

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  - M. Havranek, T. Benka, M. Hejtmanek, *et al.*, "X-CHIP-03: SOI MAPS radiation sensor with hit-counting and ADC mode", in *2018 IEEE NUCLEAR SCIENCE SYMPOSIUM AND MEDICAL IMAGING CONFERENCE PROCEEDINGS (NSS/MIC)*, IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Sydney, AUSTRALIA, NOV 10-17, 2018, IEEE Nucl & Plasma Sci Soc; IEEE, 2018, ISBN: 978-1-5386-8494-8
  - M. Marcisovska, T. Benka, M. Finger, *et al.*, "A study of single event effects induced by heavy charged particles in 180 nm SoI technology", in *2018 IEEE NUCLEAR SCIENCE SYMPOSIUM AND MEDICAL IMAGING CONFERENCE PROCEEDINGS (NSS/MIC)*, IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), Sydney, AUSTRALIA, NOV 10-17, 2018, IEEE Nucl & Plasma Sci Soc; IEEE, 2018, ISBN: 978-1-5386-8494-8

- M. Havranek, T. Benka, M. Hejtmanek, *et al.*, "MAPS sensor for radiation imaging designed in 180 nm SOI CMOS technology", *JOURNAL OF INSTRUMENTATION*, vol. 13, 2018, 19th International Workshop on Radiation Imaging Detectors (IWORID), AGH Univ Sci & Technol, Krakow, POLAND, JUL 02-06, 2017, ISSN: 1748-0221. DOI: `10.1088/1748-0221/13/06/C06004`

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